Study and Comparison of various Digital Control Techniques for DC-DC Converters

Thesis submitted in partial fulfillment of the requirements for the degree of

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in

Electrical Engineering
(Specialization: Control & Automation)

by

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Certificate

This is to certify that the work in the thesis entitled "Study and Comparison of various Digital Control Techniques for DC-DC Converters" by Rahul Verma is a record of an original research work carried out by him under my supervision and guidance in partial fulfillment of the requirements for the award of the degree of Master of Technology with the specialization of Control & Automation in the department of Electrical Engineering, National Institute of Technology Rourkela. Neither this thesis nor any part of it has been submitted for any degree or academic award elsewhere.

Place: NIT Rourkela
Date: May, 2015

Prof. Susovon Samanta
Professor, EE Department
NIT Rourkela, Odisha

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Abstract

Recent years have seen enormous amount of research and development in designing a highly efficient power supply that has good transient performance. In present scenario portable hand held applications have been dominated by integrated power supply management. In this thesis voltage mode control and current mode control of DC-DC converter has been presented. The overall design of a closed loop DC-DC converter is divided into the following different parts. First of all design of open loop Buck or Boost converter, state space analysis of the converter to find the open loop transfer function, and design of the compensator. State space averaging and then linearization is applied to obtain the small signal model of the converter to derive the various transfer functions. After obtaining the control to output transfer function, a compensator is designed to stabilize the closed loop response of the system. Normally, the compensator is designed in in analog domain and then it is transformed into equivalent discrete domain by using some transformation method like Backward Euler method, Bilinear method or pole-zero matching etc. Z-domain transfer function of the converter and modulator is needed for designing a digital controller directly. In the feedback loop, an analog to digital converter (ADC) is used before the compensator and a digital pulse width modulator (PWM) is used after the compensator. For Zeigler-Nichols tuned PID controllers a new tuning method is introduced for fast transient response and application requiring precise control. The performance of the system having auto-tuned PID controller is improved as compared to Z-N tuned PID controllers and robustness and the dead time is controlled by changing the parameter of the controller. Current mode control is used to improve the dynamic response of the system. Normally, there are two control loop in the current mode control, one is voltage control loop and another is current control loop. There are different type of digital current mode control techniques like peak current mode control, average current mode control and valley current mode control. The dynamic response of current mode control is better than voltage mode control.

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List of Abbreviations

AC: Alternating Current

BW: Bandwidth

CCM: Continuous Conduction Mode

D: Duty ratio

DC: Direct Current

DCM: Discontinuous Conduction Mode

CMC: Current Mode Control

DPWM: Digital Pulse Width Modulator

ESR: Effective Series Resistance

GCF: Gain Cross-over Frequency

GM: Gain Margin

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

PCF: Phase Cross-over Frequency

PM: Phase Margin

PWM: Pulse Width Modulator

VMC: Voltage Mode Control

ZOH: Zero Order Hold

CHAPTER 1

Introduction

1.1 Background

From the last decade the power electronic converter related to DC energy source came into focus with the increasing worldwide interest in the electronic gadgets like computer, cellphone, digital sound system and home appliance. These electronic gadgets requires different power supply, voltage and current rating. A suitable voltage regulator is required for the power supply of these electronics gadgets. A DC-DC converter is required to produce a constant stable DC output voltage while the input voltage and load current is varies. Earlier the implementation of the control of switched mode power supplies had been done using analog components due to high bandwidth and low cost. The need of fast regulation has increased with the increasing performance in the electronic circuitry. This requirement paved a way for designing higher functionality based on digital control of power converters. The digital control is having a lot of advantages over analog control like better noise immunity, flexibility of programming, easy to configure for different applications, low cost of implementation, low aging factor and ability to implement complex control algorithms. By controlling the gate pulse of the MOSFET, the closed loop control regulates the output voltage. The gate pulse of MOSFET is generated by the pulse width modulator (PWM) and PWM duty cycle is controlled by the PID controller. The closed loop control of the DC-DC converter can be operated either in voltage mode or current mode. In voltage mode control signal generated by voltage feedback loop is compared with a fixed frequency external ramp to generate the gate pulse of MOSFET while in current mode control the controlled output voltage generated by outer loop is used as reference current for the inner loop and inductor current is compared with the reference current to generate the gate pulse of the MOSFET. Most of the closed loop DC-DC converters are employ the voltage mode feedback control but the current mode feedback control preferred over voltage mode feedback control because of fast inner current loop.

1.2 Motivation

The digital controllers are the only solution in the industrial power supply production area. Nowadays Uninterruptible power supplies (UPSs) and adjustable speed drives (ASDs) are digitally controlled. One of the main consideration for DC-DC converter is to improve the efficiency of converter and to produce a constant output voltage in spite of fluctuation the input voltage and load current. Therefore in spite of operating the MOSFET in active region, it is operated in saturation and cut-off region as a switch and the control signal of the transistor is binary in nature. During the ON time of the MOSFET the voltage across the transistor is low therefore power loss is low. During the OFF time of MOSFET the current in the MOSFET is low therefore power loss is low. In the converter resistors are avoided and inductor and capacitors are used to obtain low loss. By using the digital control the output response improves as compared to analog control methods. By using the digital control auto-tuning and self-analysis strategies can be implemented which can take care of parameter variation, nonlinearities and construction tolerance of the system. The software based digital control is having a lot of advantages like better noise immunity, flexibility of programming, easy to configure for different applications, low cost of implementation, low aging factor and ability to implement complex control algorithms.

1.3 Objective

The objective of this thesis has been formulated from the above motivations. The main objective of the thesis has been categorized and is given below:

- To study the insight of DC-DC converters and develop the small signal modelling of converters to find the open loop transfer function of the DC-DC converters.
- To develop a voltage mode digital closed loop control for the buck and boost converter and study the effect of sampling in the digital control. Also a comparative study between digital control and analog control algorithms.
- Implementation of an auto-tuning control algorithm for fast varying input voltage and load current.
- Implementation of current mode control to improve the dynamic response of the system.

1.4 Literature Review

A lot of efforts has been devoted to design a digitally controlled DC-DC converter [1]-[6]. These papers are about the design of digital compensator for the voltage mode control or current mode control. For designing digital compensator an equivalent s-domain small signal model for converters with voltage mode digital control has been proposed [5]-[7]. It is a practical way to design the feedback control system for voltage mode DC-DC converters. Since Laplace-domain model of DC-DC converters with analog control is very familiar among most of the engineers, analog techniques are used to design the controller. Therefore, this type of digital controller design technique is used which unified the intuitiveness of analog control design [8]-[11]. However, first of all the controller should be designed in Laplace-domain and then Laplace-domain transfer function of compensator is mapped into z-domain by approximation methods. The continuous Laplace-domain transfer function can be easily translated into discrete equivalent by using Backward Euler method, Bilinear method and pole-zero matching. Z-domain transfer function of the converter and modulator is needed for designing a digital controller directly. Small signal analysis of digitally controlled converters in z-domain is required to find the transfer function of converter and modulator in z-domain [12]. There are two nonlinear effects of digitally controlled DC-DC converters: modulation effect and quantization effect. Due to modulation effect there is a delay in the feedback of the system. The drawback of the modulator can be improved by using Laplace and frequency domain models for uniformly sampled pulse width modulator (PWM). Due to quantization effect there is a steady- state limit cycle in digitally controlled PWM converters. By applying suitable constraints on the quantization resolution and control law the steady state limit cycle in the output can be eliminated [13]-[14]. Digital control using Digital signal processors allows implementation of flexibility of quick change in design parameter, more functional control methods and single hardware design for multiple system.

The first PI controller was introduced by Foxboro in 1934-1935. However, PI controllers can over-correct errors and cause closed-loop instability. This happens when the controller reacts too fast and too aggressively; it creates a new set of errors, even opposite to the real error. This is known as “hunting” problem. In 1942, Taylor Instrument Company’s Ziegler and Nichols introduced Ziegler-Nichols (Z-N) tuning rules. Their well-known paper “Optimum settings for automatic controllers”, presented two procedures for establishing the appropriate parameters for

PID controllers. However, the PID controller was not popular at that time, as it was not a simple concept; the parameters the manufacturers required to be tuned did not make much sense to the users. The involvement of digital computer for controlling purpose in process control industry came into account in the 1960s. On 15th march 1959, the implementation of closed loop control by a digital computer has been done in Texaco's Port Arthur plant. Afterwards a lot of research has been done in the field of digital PID controller and the implementation of digital PID controller in microprocessor has been done [15]. Digital control is having a lot of advantages like better noise immunity, flexibility of programming, easy to configure for different applications, low cost of implementation, low aging factor and ability to implement complex control algorithms.

The Z-N tuning of PID controllers is not useful for fast transient response and application requiring precise control. To overcome this problem some modification has been made in Zeigler-Nichols tuning method [16]. For Zeigler-Nichols tuned PID controllers a new auto-tuning method is presented for nonlinear and higher order system with fast transient response [17]. The performance of the system having auto-tuned PID controller is improved as compare to Z-N tuned PID controllers and robustness and the dead time is controlled by changing the parameter of the controller.

Most of the closed loop DC-DC converters are employ the voltage mode feedback control but the current mode feedback control preferred over voltage mode feedback control because of fast inner current loop [18]. Different type of digital current mode control techniques like peak current mode control, average current mode control and valley current mode control are implemented [19-21]. The dynamic response of current mode control is better than voltage mode control.

CHAPTER 2

Small Signal Modeling of DC-DC Converter

2.1 Buck Converter

Buck converter is used to step down the input voltage. The general configuration of open loop asynchronous buck converter is shown in Fig.2.1. Asynchronous buck converter can be converted into synchronous buck converter by replacing the diode with an identical MOSFET and the controlling pulse of this MOSFET will be 180̊ out of phase with the controlling pulse of the first MOSFET.

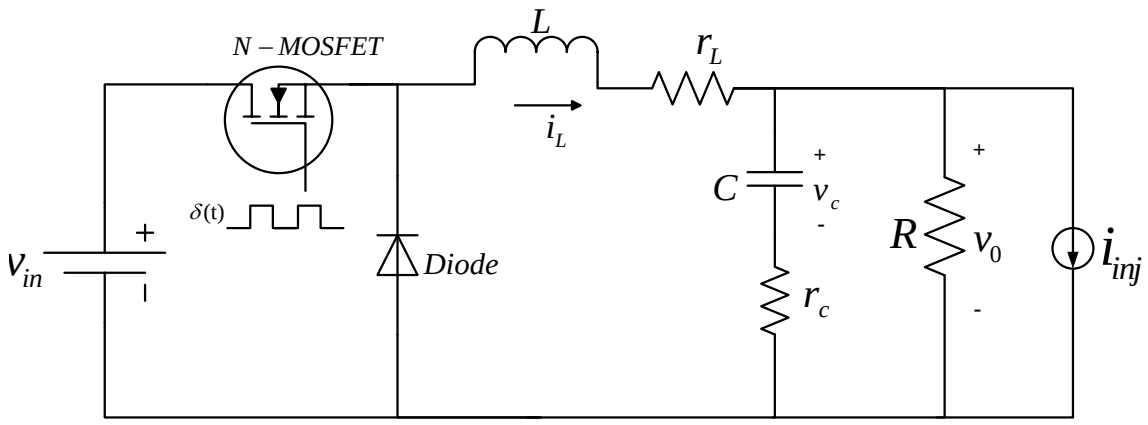

Fig. 2.1 Circuit diagram of open loop asynchronous Buck converter

For the system to be in continuous conduction mode (CCM), specific value of capacitor and inductor are required. To determine the value of inductor (L) and capacitor (C) applied input voltage (V_{in}) and nominal output voltage (V_0) is required.

Due to very high switching frequency of the MOSFET in the Buck converter the switch produces discontinuous current but the inductor keeps the output current continuous. During ON state of the MOSFET an electric current flows from source to load and inductor gets charged. During OFF state of the MOSFET no electric current flows from source to load. In this state the inductor acts as a source and releases its stored energy i.e. inductor discharges, hence there is a

current flow from inductor to load. The inductor current i_L in CCM is shown in Fig.2.2. The inductor current should never reach zero value in the continuous conduction mode.

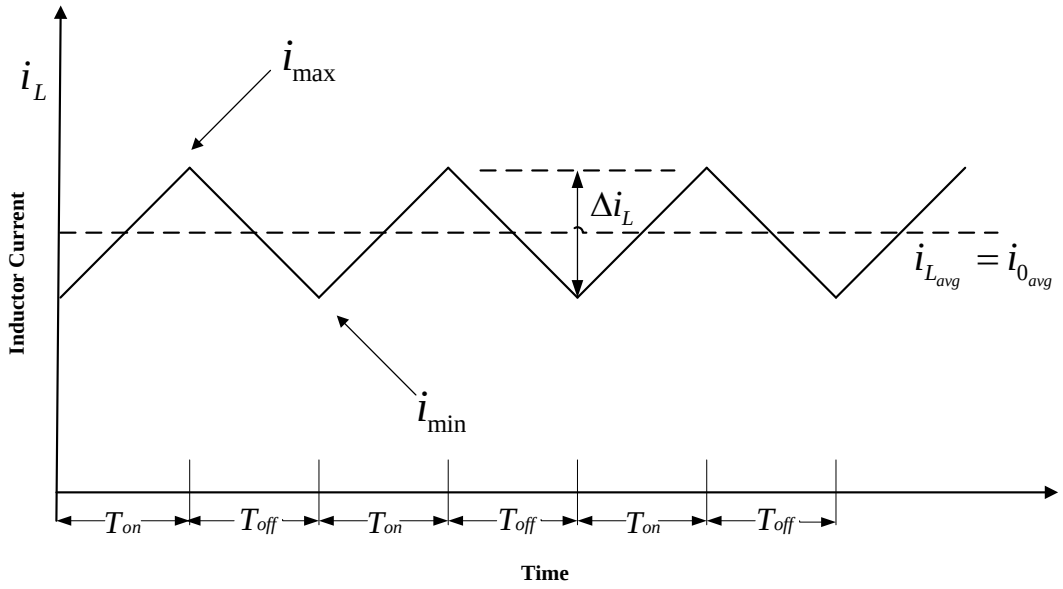

Fig. 2.2 Inductor current of Buck converter in steady state

From the fig. 2.2 it can be seen that the inductor current varies between a maximum current $i_{\max}$ and minimum current $i_{\min}$ and the difference between maximum and minimum current is peak to peak inductor current ripple Δi_L. In steady state the average inductor current i_{Lavg} is equal to average output current i_{0avg}. The inductor current should never exceed the saturation current otherwise there will be instantaneous increase in the inductor current and insignificant inductance loss. The key factor for choosing the inductor value is peak to peak inductor current Δi_L. The peak to peak inductor current should be 30-40% of average output current i_{0avg}. The equation for finding inductor value L in CCM is given below.

$$L = \frac{V_0 \left(1 - D_{\min}\right) T}{\Delta I_{L\max}} \tag{2.1}$$

Where,

- V_0 Average output voltage (Volt)
- $\Delta I_{L\max}$ Maximum inductor ripple current (Amp.)

- T Switching time period (Sec.)
- $D_{\min}$ Minimum duty ratio

The capacitor maintains constant output voltage and makes output voltage ripple free. In practical there is always an equivalent series resistance (ESR) present with the capacitor. The capacitor should be selected with minimum ESR. For certain output voltage ripple the maximum ESR of the capacitor and the capacitor value can be calculated with the following equations.

$$ESR = \frac{V_{0ripple}}{\Delta I_L} \tag{2.2}$$

$$C = \frac{\Delta I_L T}{8 \Delta V_c} \tag{2.3}$$

Where,

- $V_{0ripple}$ Output voltage ripple (Volt)
- ΔI_L Inductor current ripple (Amp.)
- ΔV_c Capacitor voltage ripple (Volt)

2.1.1 Derivation of State Equations

There are two different system configuration of buck converter in CCM are considered, one during ON time of MOSFET and another during OFF time of the MOSFET. The circuit diagram of buck converter during ON time of MOSFET is shown in Fig. 2.3.

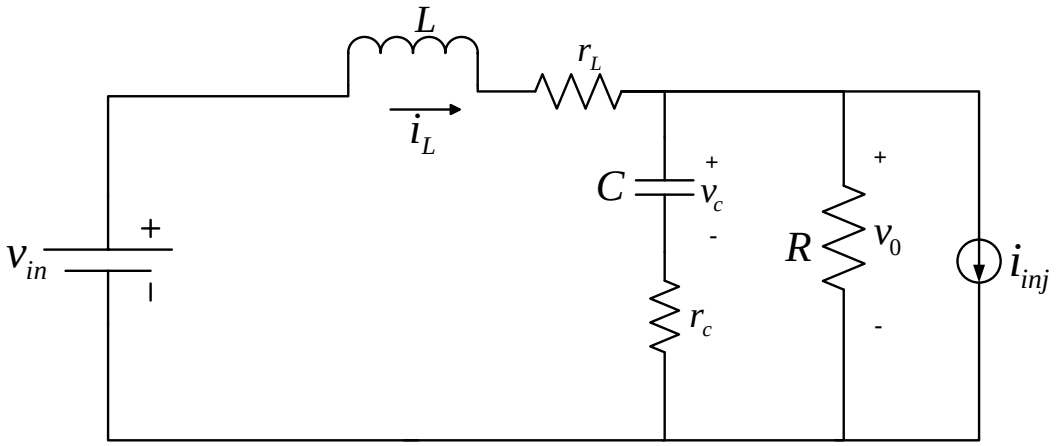

Fig. 2.3 Circuit diagram of Buck converter during ON time

From Fig. 2.3 the following equations are obtained:

$$\frac{di_L}{dt} = \frac{1}{L}\left(v_{in} - v_0\right) \tag{2.4}$$

$$\frac{dv_c}{dt} = \frac{1}{C}\left(i_L - \frac{v_0}{R} - i_{inj}\right) \tag{2.5}$$

$$v_0 = v_c + R_c\left(i_L - \frac{v_0}{R} - i_{inj}\right) \tag{2.6}$$

By rearranging eq. (2.6) it can be written as:

$$v_0 + \frac{r_c}{R}v_0 = v_c + r_c\left(i_L - i_{inj}\right) \tag{2.7}$$

$$v_0 = \frac{v_c + r_c\left(i_L - i_{inj}\right)}{1 + r_c/R} \tag{2.8}$$

$$v_0 = \frac{r_c \cdot R}{r_c + R}i_L + \frac{R}{r_c + R}v_c - \frac{r_c \cdot R}{r_c + R}i_{inj} \tag{2.9}$$

On substituting the value of v_0 from eq. (2.9) in eq. (2.4) and (2.5):

$$\frac{di_L}{dt} = -\frac{r_c \cdot R}{\mathrm{L}(r_c + R)}i_L - \frac{R}{\mathrm{L}(r_c + R)}v_c + \frac{1}{L}v_{in} + \frac{r_c \cdot R_c}{\mathrm{L}(r_c + R)}i_{inj} \tag{2.10}$$

$$\frac{dv_c}{dt} = \frac{1}{C}i_L - \frac{r_c}{\mathrm{C}(r_c + R)}i_L - \frac{1}{\mathrm{C}(r_c + R)}v_c + \frac{r_c}{\mathrm{C}(r_c + R)}i_{inj} - \frac{1}{C}i_{inj} \tag{2.11}$$

On simplifying eq. (2.11) it can be written as:

$$\frac{dv_c}{dt} = \frac{R}{\mathrm{C}(r_c + R)}i_L - \frac{1}{\mathrm{C}(r_c + R)}v_c - \frac{R}{\mathrm{C}(r_c + R)}i_{inj} \tag{2.12}$$

The open loop buck converter shown in Fig. 2.1 is a second order system since it is having two energy storage component. Let the current of inductor i_L and capacitor voltage v_c be chosen as state variables. Let input voltage v_{in} and load current i_{inj} as input signals and output voltage v_0

as output signal. The state space system obtained by using eq. (2.9), (2.10), and (2.12) are as follows:

$$\begin{cases} \dfrac{dx(\mathrm{t})}{dt} = A_1 * x(\mathrm{t}) + B_1 * u(\mathrm{t}) \\ y(\mathrm{t}) = C_1 * \mathrm{x}(\mathrm{t}) + F_1 * u(\mathrm{t}) \end{cases} \tag{2.13}$$

After substituting the matrixes A_1, B_1, C_1, F_1 state variable $x(\mathrm{t})$, input signal $u(\mathrm{t})$, and output signal $y(\mathrm{t})$ in eq. (2.13):

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} -\dfrac{r_c.R}{\mathrm{L}(r_c+R)} & -\dfrac{R}{\mathrm{L}(r_c+R)} \\ \dfrac{R}{\mathrm{C}(r_c+R)} & -\dfrac{1}{\mathrm{C}(r_c+R)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & \dfrac{r_c.R}{\mathrm{L}(r_c+R)} \\ 0 & -\dfrac{R}{\mathrm{C}(r_c+R)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{inj} \end{bmatrix} \tag{2.14}$$

$$v_0 = \begin{bmatrix} \dfrac{r_c.R}{(r_c+R)} & \dfrac{R}{(r_c+R)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & -\dfrac{r_c.R}{(r_c+R)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{inj} \end{bmatrix} \tag{2.15}$$

When the MOSFET is OFF, the diode is forward bias and the diode is replaced by short circuit. The circuit diagram of buck converter during OFF time of MOSFET is shown in Fig. 2.4.

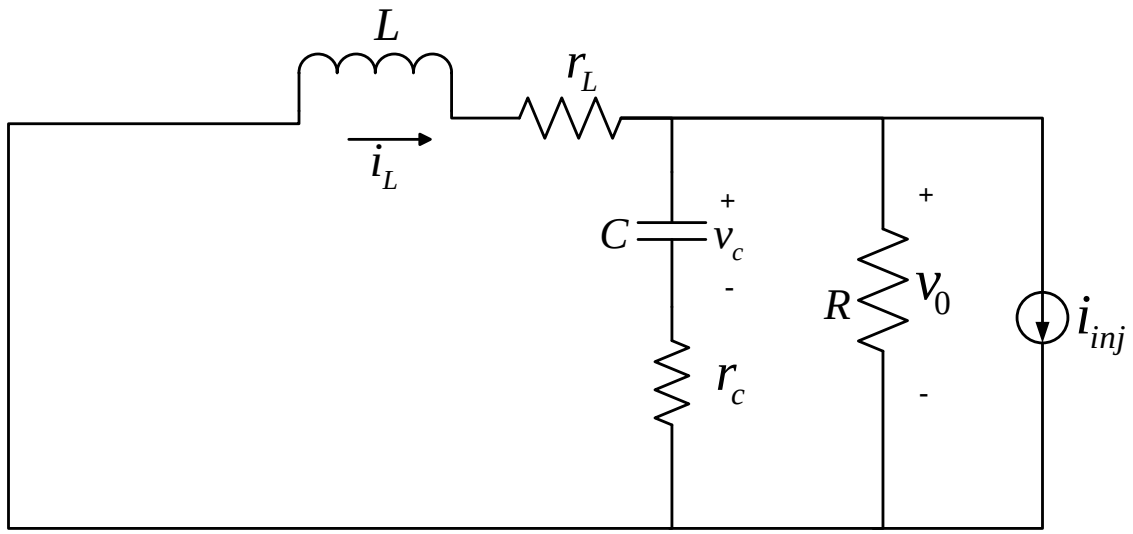

Fig. 2.4 Circuit diagram of Buck converter during OFF time

If the input voltage v_{in} is zero, the circuit of buck converter during ON time of MOSFET and OFF time of MOSFET are same. Hence the state space model of buck converter during OFF can be obtained by putting the coefficients for v_{in} to zero in eq. (2.13).

$$\begin{cases} \dfrac{dx(\mathrm{t})}{dt} = A_2 * x(\mathrm{t}) + B_2 * u(\mathrm{t}) \\ y(\mathrm{t}) = C_2 * \mathrm{x}(\mathrm{t}) + F_2 * u(\mathrm{t}) \end{cases} \tag{2.16}$$

After substituting the matrixes A_2, B_2, C_2, F_2 state variable $x(\mathrm{t})$, input signal $u(\mathrm{t})$, and output signal $y(\mathrm{t})$ in eq. (2.16):

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} -\dfrac{r_c.R}{\mathrm{L}(r_c+R)} & -\dfrac{R}{\mathrm{L}(r_c+R)} \\ \dfrac{R}{\mathrm{C}(r_c+R)} & -\dfrac{1}{\mathrm{C}(r_c+R)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{r_c.R}{\mathrm{L}(r_c+R)} \\ 0 & -\dfrac{R}{\mathrm{C}(r_c+R)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{inj} \end{bmatrix} \tag{2.17}$$

$$v_0 = \begin{bmatrix} \dfrac{r_c.R}{(r_c+R)} & \dfrac{R}{(r_c+R)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & -\dfrac{r_c.R}{(r_c+R)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{inj} \end{bmatrix} \tag{2.18}$$

2.1.2 State-Space Averaging

In continuous conduction mode the buck converter ON time and OFF time configurations are shown in Fig. 2.3 and 2.4. Let the ON time duration of the MOSFET for nth cycle is d_nT and the OFF time duration is $d_n'T = (1-d_n)T$. Where $d_n = T_{on}/T$ duty ratio of the converter. The state space equations of the converter can be written as:

$$\mathrm{T}_{on}: \quad \hat{x}(\mathrm{t}) = A_1 * x(\mathrm{t}) + B_1 * u(\mathrm{t}) \qquad for \qquad nT \le t \le nT + d_nT, \qquad n = 1, 2, \ldots\ldots \tag{2.19}$$

$$\mathrm{T}_{off}: \quad \hat{x}(\mathrm{t}) = A_2 * x(\mathrm{t}) + B_2 * u(\mathrm{t}) \qquad for \qquad nT + d_nT \le t \le (n+1)T, \qquad n = 1, 2, \ldots\ldots \tag{2.20}$$

The solution of the eq. (2.19) and (2.20) are obtained by integrating them over each period of operation.

$$x(n+d_n)T = e^{A_1 d_n T} x(nT) + A_1^{-1}\left(e^{A_1 d_n T} - I\right) B_1 u \tag{2.21}$$

$$x(n+1)T = e^{A_2 d_n' T} x(nT + d_nT) + A_2^{-1}\left(e^{A_2 d_n' T} - I\right) B_2 u \tag{2.22}$$

On substituting eq. (2.21) in (2.22):

$$x(n+1)T = e^{(A_1 d_n + A_2 d_n')T} x(nT) + A_1^{-1}\left(e^{(A_1 d_n + A_2 d_n')T} - e^{A_2 d_n' T}\right) B_1 u + A_1^{-1}\left(e^{A_2 d_n' T} - I\right) B_2 u \tag{2.23}$$

By using linear approximation $e^{AT} = 1 + AT$ eq. (2.23) is written as:

$$x(n+1)T = x(nT) + \left(A_2 d_n^{'} + A_1 d_n\right) T * x(nT) + \mathrm{d}_n TB_1 u + d_n' TB_2 u \tag{2.24}$$

$$\frac{x(n+1)T - x(nT)}{T} = \left(A_2 d_n' + A_1 d_n\right) * x(nT) + (B_1 \mathrm{d}_n + B_2 d_n')u \tag{2.25}$$

By using the forward Euler's approximation $\dot{x} = \frac{x(n+1)T - x(nT)}{T}$ eq. (2.25) is written as:

$$\dot{x} = \left(A_1 d_n + A_2 d_n'\right) x + (B_1 \mathrm{d}_n + B_2 d_n')u \tag{2.26}$$

Similarly output state equation is written as:

$$y = \left(C_1 d_n + C_2 d_n'\right) x + (F_1 d_n + F_2 d_n')u \tag{2.27}$$

2.1.3 Linearization

The linear small signal model of eq. (2.26) and (2.27) can be derived by using perturbation around a steady state point $\left(X, D, U\right)$. Let d

$$x = X + \hat{x}, d = D + \hat{d}, and\, u = U + \hat{u} \tag{2.28}$$

On substituting the value of x, d , and u from eq.2.28 in eq. (2.27) and (2.27) and separating the small signals:

$$\dot{\hat{x}} = \left(A_1 D + A_2 D'\right)\hat{x} + \left(B_1 D + B_2 D'\right)\hat{u} + \left(\left(B_1 - B_2\right)U + \left(A_1 - A_2\right)X\right)\hat{d} \tag{2.29}$$

$$\hat{y} = \left(C_1 D + C_2 D'\right)\hat{x} + \left(F_1 D + F_2 D'\right)\hat{u} \tag{2.30}$$

Let $A_1 D + A_2 D' = A, B_1 D + B_2 D' = B, C_1 D + C_2 D' = C, F_1 D + F_2 D' = F$, then eq. (2.29) and (2.30) is rewritten as:

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} + \left(\left(B_1 - B_2\right)U + \left(A_1 - A_2\right)X\right)\hat{d} \tag{2.31}$$

$$\hat{y} = C\hat{x} + F\hat{u} \tag{2.32}$$

After considering the perturbation a constant term the study state value of state variables and duty ratio are obtained and is given as:

$$\begin{aligned} AX + BU &= 0 \\ Y &= CX + FU \end{aligned} \tag{2.33}$$

By using eq. (2.33) the output variable is expressed as:

$$Y = \left(-CA^{-1}B + E\right)U \tag{2.34}$$

Let the initial state of the linearized model is zero. The Laplace transform of eq. (2.31) and (2.32) is written as:

$$s\hat{x}(\mathrm{s}) = A\hat{x}(s) + B\hat{u}(s) + \left(\left(B_1 - B_2\right)U + \left(A_1 - A_2\right)X\right)\hat{d}(s) \tag{2.35}$$

$$\hat{y}(s) = C\hat{x}(s) + F\hat{u}(s) \tag{2.36}$$

By using superposition theorem eq. (2.35) and (2.36) is simplified as:

$$\hat{\mathrm{x}}(\mathrm{s}) = \left(SI - A\right)^{-1} B\hat{u}(s) + \left(SI - A\right)^{-1}\left(\left(B_1 - B_2\right)U + \left(A_1 - A_2\right)X\right)\hat{d}(s) \tag{2.37}$$

$$\hat{y}(s) = C\left(\left(SI - A\right)^{-1} B\hat{u}(s) + \left(SI - A\right)^{-1}\left(\left(B_1 - B_2\right)U + \left(A_1 - A_2\right)X\right)\hat{d}(s)\right) + F\hat{u}(s) \tag{2.38}$$

By substituting the state space matrixes A, B, C, and F of buck converter in eq. (2.38), the following transfer functions are obtained for open loop power stage:

$$G_{v_0 d}(s) = \frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{v_{in}R\left(1 + sr_cC\right)}{s^2\left(R + r_c\right)LC + s\left(L + r_cRC\right) + R} \tag{2.39}$$

$$G_{v_0 v_{in}}(s) = \frac{\hat{v}_0(s)}{\hat{v}_{in}(s)} = \frac{RD\left(1 + sr_cC\right)}{s^2\left(R + r_c\right)LC + s\left(L + r_cRC\right) + R} \tag{2.40}$$

$$G_{v_0 i_{inj}}(s) = \frac{\hat{v}_0(s)}{\hat{i}_{inj}(s)} = -\frac{sRL\left(1 + sr_cC\right)}{s^2\left(R + r_c\right)LC + s\left(L + r_cRC\right) + R} \tag{2.41}$$

$$G_{i_L d}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{v_{in}\left(1 + s\left(R + r_c\right)C\right)}{s^2\left(R + r_c\right)LC + s\left(L + r_cRC\right) + R} \tag{2.42}$$

$$G_{i_L v_{in}}(s) = \frac{\hat{i}_L(s)}{\hat{v}_{in}(s)} = \frac{D\left(1+s\left(R+r_c\right)C\right)}{s^2\left(R+r_c\right)LC+s\left(L+r_cRC\right)+R} \tag{2.43}$$

$$G_{i_L i_{inj}}(s) = \frac{\hat{i}_L(s)}{\hat{i}_{inj}(s)} = \frac{R\left(1+sr_cC\right)}{s^2\left(R+r_c\right)LC+s\left(L+r_cRC\right)+R} \tag{2.44}$$

The block diagram of the buck converter in terms of the transfer function is shown in Fig. 2.5.

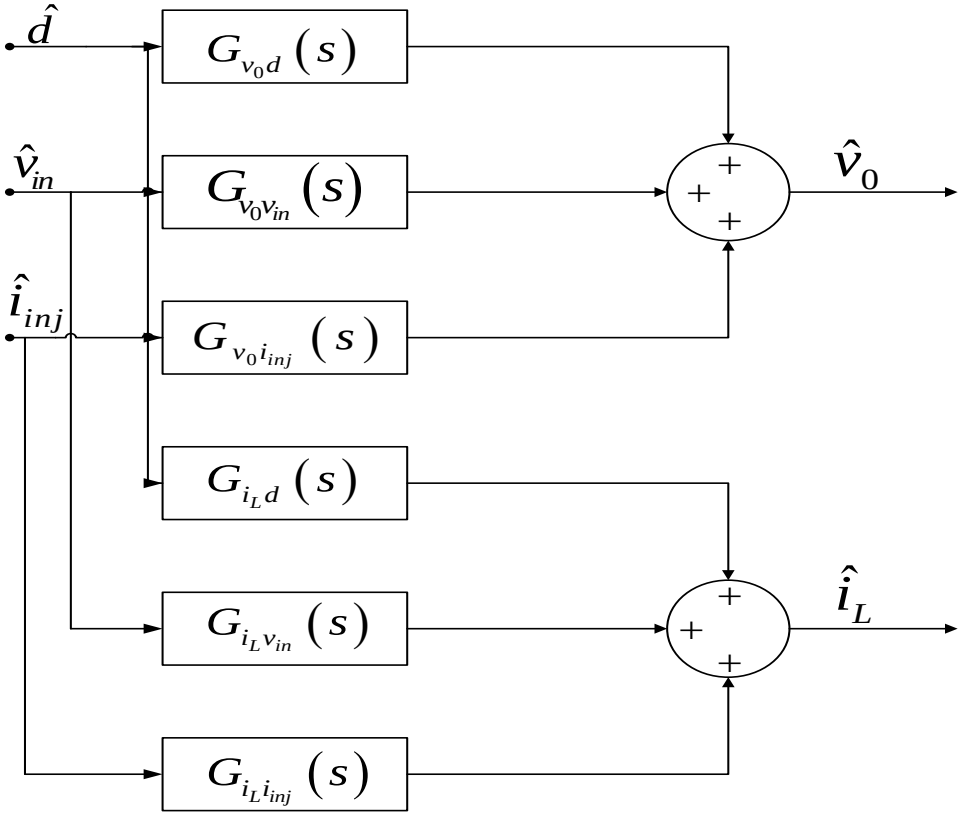

Fig. 2.5 Block diagram of the open loop power stage of Buck converter

2.2 Boost Converter

Boost converter is used to step-up the DC input voltage. The general configuration of open loop asynchronous boost converter is shown in Fig. 2.6. The asynchronous boost converter can be converted into synchronous boost converter by replacing the diode with another similar MOSFET and the gate pulse of the second MOSFET will be 180^0 out of phase with the first MOSFET gate pulse.

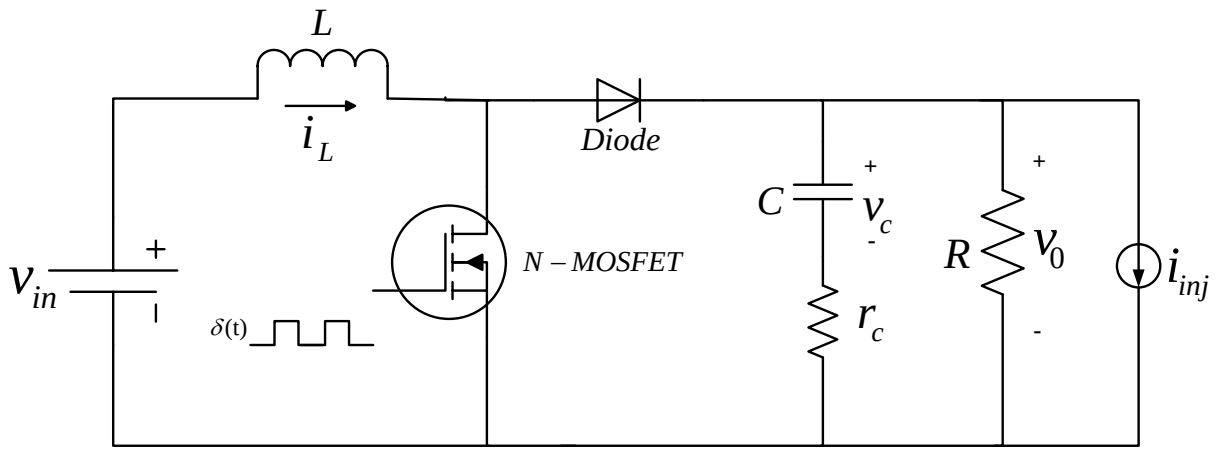

Fig. 2.6 Circuit diagram of open loop asynchronous Boost converter

For the system to be in continuous conduction mode (CCM), specific value of capacitor and inductor are required. To determine the value of inductor (L) and capacitor (C) applied input voltage (V_{in}) and nominal output voltage (V_0) is required.

Due to very high switching frequency of the MOSFET in the Boost converter the switch produces discontinuous current but capacitor keeps output current continuous. During OFF state of the MOSFET an electric current flows from source to load and capacitor gets charged. During ON state of the MOSFET no electric current flows from source to load. In this state the capacitor acts as a source and releases its stored energy i.e. capacitor discharges, hence there is a current flow from capacitor to load. The capacitor voltage v_c in CCM is shown in Fig.2.7. In continuous conduction mode the capacitor voltage never reaches to zero value.

From Fig. 2.7 it can be seen that the capacitor voltage varies between $v_{\max}$ and $v_{\min}$ and the difference between the maximum and minimum voltage is peak-to-peak capacitor voltage ripple Δv_c. The capacitor voltage should never exceed the saturation voltage otherwise there will be instantaneous increase in output current.

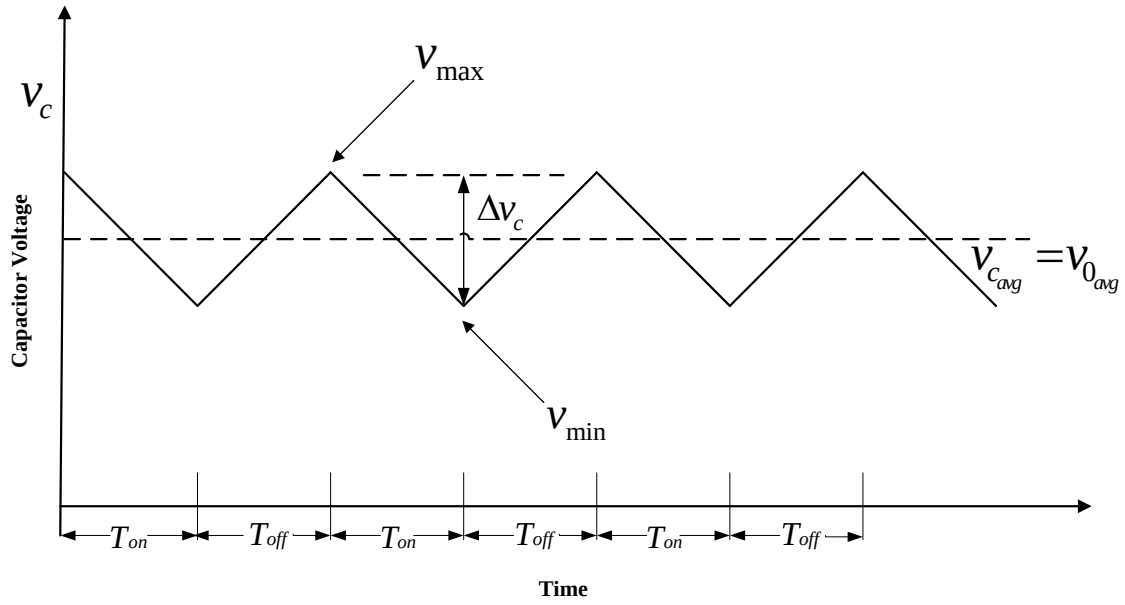

Fig. 2.7 Capacitor current of Boost converter in steady state

The equation for finding the value of capacitance C in CCM is given below:

$$C = \frac{v_0 DT}{\Delta v_c R} \tag{2.45}$$

Where,

- v_0 Output voltage (Volt)
- Δv_c Capacitor voltage ripple (Volt)
- D Duty cycle
- T Switching time period (Sec.)

The equation for finding the value of inductance L in CCM is giver below:

$$L = \frac{v_0 D(1-D)T}{\Delta i_L} \tag{2.46}$$

Where,

- Δi_L Inductor current ripple (Amp.)
- v_0 Output voltage (Volt)
- T Switching time period (Sec.)

2.2.1 Derivation of state equations

There are two different system configuration of boost converter in CCM are considered, one during ON time of MOSFET and another during OFF time of the MOSFET. The circuit diagram of boost converter during ON time of MOSFET is shown in Fig. 2.8.

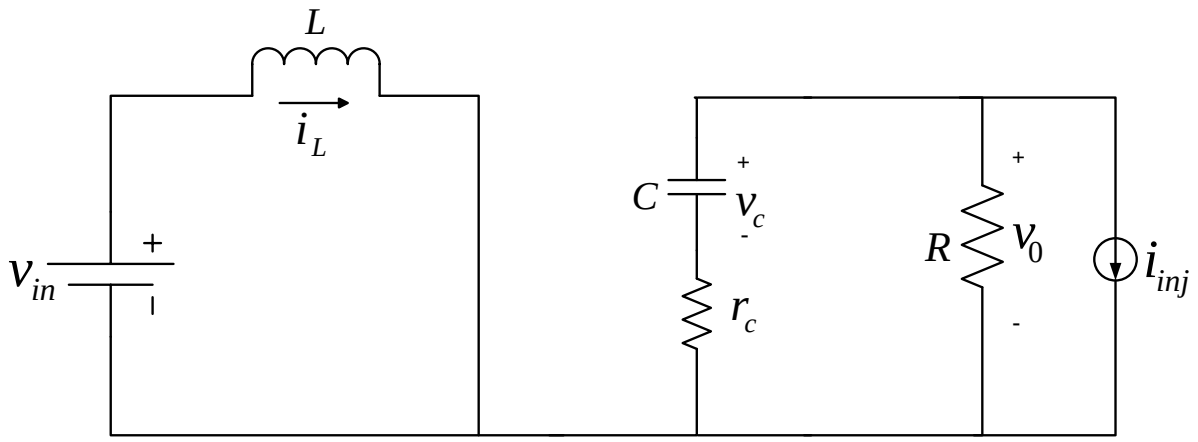

Fig. 2.8 Circuit diagram of Boost converter during ON time

From Fig. 2.8 the following equations are obtained:

$$\frac{di_L}{dt} = \frac{1}{L} v_{in} \tag{2.47}$$

$$\frac{dv_c}{dt} = \frac{1}{C}\left(-\frac{v_0}{R} - i_{inj} \right) \tag{2.48}$$

$$v_0 = v_c + r_c\left(-\frac{v_0}{R} - i_{inj} \right) \tag{2.49}$$

By rearranging eq. (2.49) it can be written as:

$$v_0 + \frac{r_c}{R} v_0 = v_c - r_c i_{inj} \tag{2.50}$$

$$v_0 = \frac{v_c - r_c i_{inj}}{1 + r_c / R} \tag{2.51}$$

$$v_0 = \frac{R}{r_c + R} v_c - \frac{r_c R}{r_c + R} i_{inj} \tag{2.52}$$

After substituting the value of v_0 from eq. (2.52) to (2.48):

$$\frac{dv_c}{dt} = -\frac{1}{C\left(r_c + R\right)} v_c + \frac{r_c}{R\left(r_c + R\right)} i_{inj} - \frac{1}{C} i_{inj} \tag{2.53}$$

On simplifying the eq. (2.53) it can be written as:

$$\frac{dv_c}{dt} = -\frac{1}{C\left(r_c + R\right)} v_c - \frac{R}{C\left(r_c + R\right)} i_{inj} \tag{2.54}$$

The open loop boost converter shown in Fig. 2.7 is a second order system since it is having two energy storage component. Let the current of inductor i_L and capacitor voltage v_c be chosen as state variables. Let input voltage v_{in} and load current i_{inj} as input signals and output voltage v_0 as output signal. The state space system obtained by using eq. (2.47), (2.52), and (2.54) are as follows:

$$\begin{cases} \dfrac{dx(\mathrm{t})}{dt} = A_1 * x(\mathrm{t}) + B_1 * u(\mathrm{t}) \\ y(\mathrm{t}) = C_1 * \mathrm{x}(\mathrm{t}) + F_1 * u(\mathrm{t}) \end{cases} \tag{2.55}$$

After substituting the matrixes A_1, B_1, C_1, F_1 state variable $x(\mathrm{t})$, input signal $u(\mathrm{t})$, and output signal $y(\mathrm{t})$ in eq. (2.55):

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{\mathrm{C}(r_c + R)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & 0 \\ 0 & -\dfrac{R}{\mathrm{C}(r_c + R)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{inj} \end{bmatrix} \tag{2.56}$$

$$v_0 = \begin{bmatrix} 0 & \dfrac{R}{(r_c + R)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & -\dfrac{r_c . R}{(r_c + R)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{inj} \end{bmatrix} \tag{2.57}$$

When the MOSFET is OFF, the diode is forward bias and the diode is replaced by short circuit. The circuit diagram of boost converter during OFF time of MOSFET is shown in Fig. 2.9.

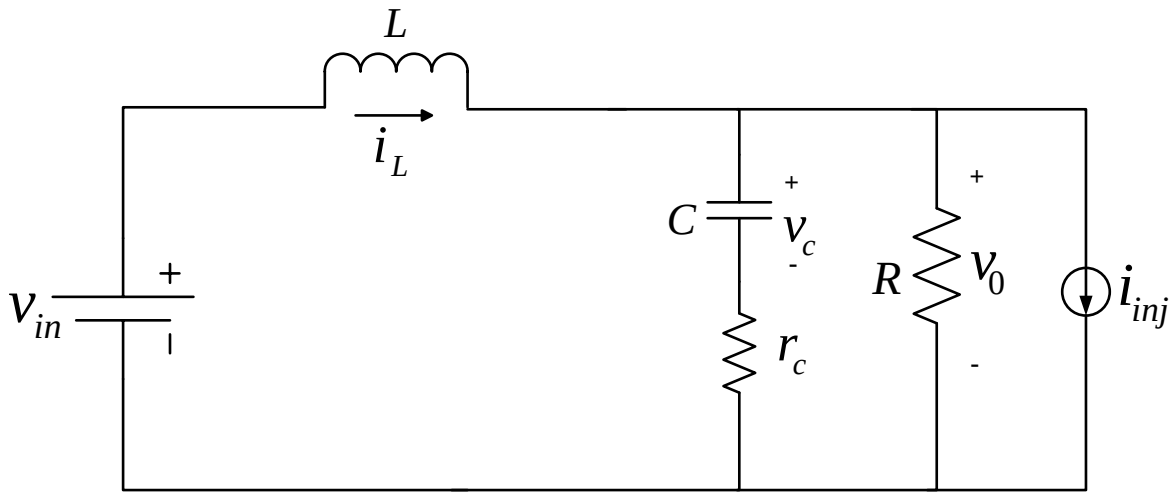

Fig. 2.9 Circuit diagram of Boost converter during OFF time

The circuit of boost converter during OFF time is same as the circuit of buck converter during ON time. Hence it can be used as model of boost converter during OFF time. By using eq. (2.13), (2.14), and (2.15) the state space model of boot converter during OFF time is given as:

$$\begin{cases} \dfrac{dx(\mathrm{t})}{dt} = A_1 * x(\mathrm{t}) + B_1 * u(\mathrm{t}) \\ y(\mathrm{t}) = C_1 * \mathrm{x}(\mathrm{t}) + F_1 * u(\mathrm{t}) \end{cases} \tag{2.58}$$

After substituting the matrixes A_1, B_1, C_1, F_1 state variable $x(\mathrm{t})$, input signal $u(\mathrm{t})$, and output signal $y(\mathrm{t})$ in eq. (2.58):

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} -\dfrac{r_c.R}{\mathrm{L}(r_c+R)} & -\dfrac{R}{\mathrm{L}(r_c+R)} \\ \dfrac{R}{\mathrm{C}(r_c+R)} & -\dfrac{1}{\mathrm{C}(r_c+R)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & \dfrac{r_c.R}{\mathrm{L}(r_c+R)} \\ 0 & -\dfrac{R}{\mathrm{C}(r_c+R)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{inj} \end{bmatrix} \tag{2.59}$$

$$v_0 = \begin{bmatrix} \dfrac{r_c.R}{(r_c+R)} & \dfrac{R}{(r_c+R)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 & -\dfrac{r_c.R}{(r_c+R)} \end{bmatrix} \begin{bmatrix} v_{in} \\ i_{inj} \end{bmatrix} \tag{2.60}$$

By substituting the state space matrixes A, B, C, and F of boost converter in eq. (2.38), the following transfer functions are obtained for open loop power stage:

$$G_{v_0 d}(s)=\frac{\hat{v}_0(s)}{\hat{d}(s)}=\frac{\left(v_{in}/\left(D'\left(r_c+RD'\right)\right)\right)\left(R^2D'^2-sL\left(r_c+R\right)\right)\left(1+sCr_c\right)}{s^2LC\left(r_c+R\right)+s\left(r_cRCD'+L\right)+RD'\left(r_c+RD'\right)/\left(r_c+R\right)} \tag{2.61}$$

$$G_{v_0 v_{in}}(s)=\frac{\hat{v}_0(s)}{\hat{v}_{in}(s)}=\frac{RD'\left(1+sCr_c\right)}{s^2LC\left(r_c+R\right)+s\left(r_cRCD'+L\right)+RD'\left(r_c+RD'\right)/\left(r_c+R\right)} \tag{2.62}$$

$$G_{v_0 i_{inj}}(s)=\frac{\hat{v}_0(s)}{\hat{i}_{inj}(s)}=-\frac{\left(1+sCr_c\right)\left(\left(r_cR^2DD'/\left(r_c+R\right)\right)+sLR\right)}{s^2LC\left(r_c+R\right)+s\left(r_cRCD'+L\right)+RD'\left(r_c+RD'\right)/\left(r_c+R\right)} \tag{2.63}$$

$$G_{i_L d}(s)=\frac{\hat{i}_L(s)}{\hat{d}(s)}=\frac{\frac{v_{in}}{D'}\left(1+\frac{RD'}{\left(r_c+RD'\right)}+sC\left(r_c+R\right)\right)}{s^2LC\left(r_c+R\right)+s\left(r_cRCD'+L\right)+RD'\left(r_c+RD'\right)/\left(r_c+R\right)} \tag{2.64}$$

$$G_{i_L v_{in}}(s)=\frac{\hat{i}_L(s)}{\hat{v}_{in}(s)}=\frac{1+sC\left(r_c+R\right)}{s^2LC\left(r_c+R\right)+s\left(r_cRCD'+L\right)+RD'\left(r_c+RD'\right)/\left(r_c+R\right)} \tag{2.65}$$

$$G_{i_L i_{inj}}(s)=\frac{\hat{i}_L(s)}{\hat{i}_{inj}(s)}=\frac{RD'\left(1+sCr_c\right)}{s^2LC\left(r_c+R\right)+s\left(r_cRCD'+L\right)+RD'\left(r_c+RD'\right)/\left(r_c+R\right)} \tag{2.66}$$

CHAPTER 3

Digital Feedback Control

Nowadays the controllers are exclusively being implemented in digital domain. In digital controllers the microprocessor and encoders are used in place of mechanical integrator and differentiator in analog controllers. The implementation of microprocessor based control is less expensive than its analog counterpart. Digital control allows implementation of flexibility of quick change in design parameter, more functional control methods and single hardware design for multiple system. Due to its speed, versatility, simplicity, reliability, robustness, and flexibility, most of the industries rely on digital controller for all types of control. Further, the interfacing between a digital controller and other digital hardware is very easy. Most of the dynamic system in industries are continuous in nature in spite of discrete. Hence, the output signal of the system is required to be processed before using in microprocessor. An analog to digital converter is required to process the output signal of the system from analog to discrete domain. In the same way the output of the microprocessor is required to be convert in analog domain from discrete domain before applying to the system. The block diagram of digitally controlled DC-DC converter is shown in Fig. 3.1.

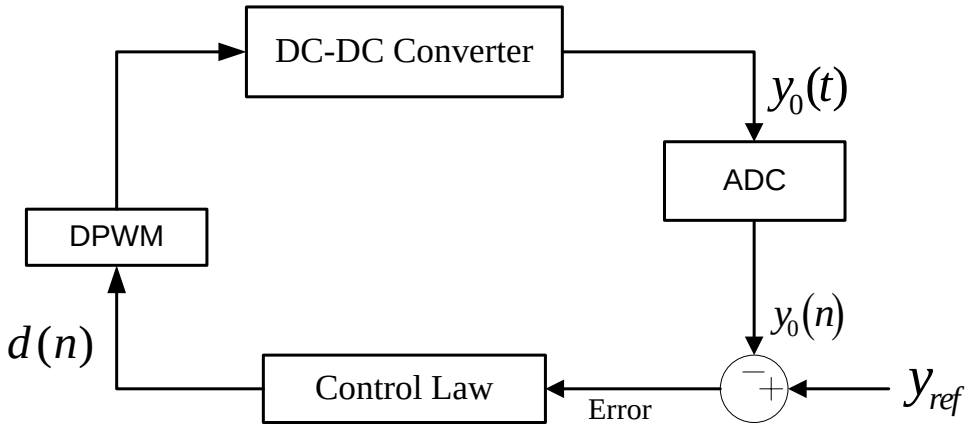

Fig. 3.1 Block diagram of closed loop DC-DC converter

As shown in the above diagram the output of DC-DC converter is converted to discrete signal by using ADC and the output of the controller is given to digital pulse width modulator to generate the control signal. The structure of a discrete time PID control law is given below:

$$d(n) = K_p\left(e(n) - e(n-1)\right) K_d\left(e(n) + e(n-2) - 2e(n-1)\right) + K_i \Delta T_s e(n) + d(n-1) \quad (3.1)$$

Where, K_p is proportional gain, K_d is derivative gain, K_i is integral gain, $e(n)$ is the error signal and $d(n)$ id duty cycle at time n.

$$e(n) = y_{ref}(n) - y_0(n) \quad (3.2)$$

Where, $y_{ref}(n)$ is the reference signal and $y_0(n)$ is the digital representation of the output of the plant.

3.1 Pulse Width Modulator

PWM provides an intermediate amount of electric power between fully OFF and fully ON. The output of the PWM circuit is a square wave with varying ON and OFF time. Duty cycle is defined as ON time (T_{on}) to time period (T) ratio of the PWM output signal. The analog implementation of PWM is given below:

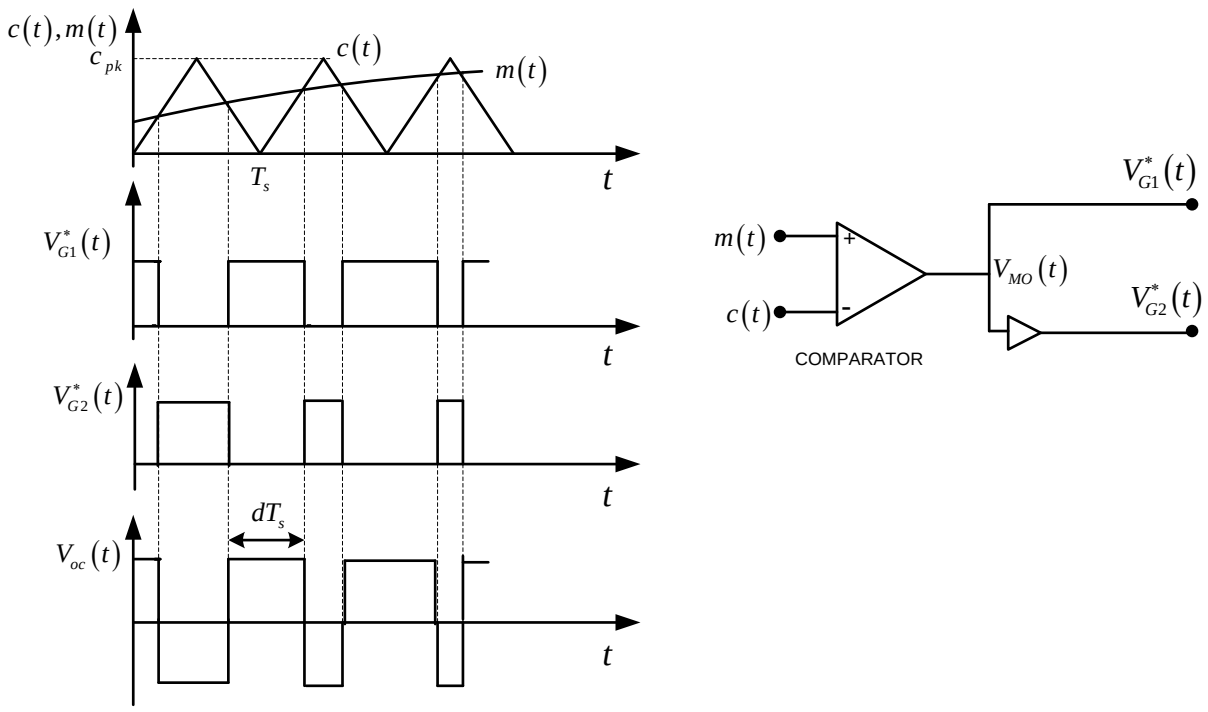

Fig. 3.2 Naturally sampled implementation of a PWM modulator

As shown in the Fig. 3.2 the controlled output of the compensator $m(t)$ and a triangular pulse $c(t)$ is applied to the input of the compensator. The duty ratio of the PWM output signal depends on the amplitude of the $m(t)$. We can explicitly relate signal $m(t)$ to the resulting PWM duty-cycle. Simple calculations show that, in each modulation period, where a constant m is assumed, the following equation holds:

$$\frac{m}{dT_s} = \frac{c_{pk}}{T_s} \qquad \langle = \rangle \qquad d = \frac{m}{c_{pk}} \tag{3.3}$$

The above result is correct only if the modulating signal changes slowly along time, with respect to the carrier signal, i.e. the upper limit of $m(t)$ bandwidth is well below. This means that, in the hypothesis of a limited bandwidth $m(t)$, the information carried by this signal is transferred by the PWM process to the duty-cycle that will change slowly along time following the evolution. Based on the previous relation, it means that:

$$\frac{\partial d}{\partial m} = \frac{1}{c_{pk}} \tag{3.4}$$

The duty-cycle, in turn, is transferred to the load voltage waveform by the power converter. The slow variations of the load voltage average value will therefore copy those of signal $m(t)$. Therefore, the modulator transfer function, including the inverter gain will be given by:

$$\frac{\partial \overline{V}_{oc}}{\partial m} = \frac{\partial \overline{V}_{oc}}{\partial d}\frac{\partial d}{\partial m} = \frac{2V_{DC}}{c_{pk}} \tag{3.5}$$

3.1.1 Dynamic response of analog PWM modulator

Indeed, it is possible to see that any change in the modulating signal's amplitude, provided that its bandwidth limitation is maintained, implies an "immediate", i.e. in phase, adjustment of the resulting duty-cycle. This means that the analog implementation of PWM guarantees the minimum delay between modulating signal and duty-cycle.

The dynamic response of analog PWM modulator is shown in Fig. 3.3. Where, the modulating signal $m(t)$ is decomposed in a dc component M and a small signal perturbation $\tilde{m}$ $\left(i.e. m(t) = M + \tilde{m}\right)$. The corresponding duty-cycle has been found, whose small signal component is called $\tilde{d}$.

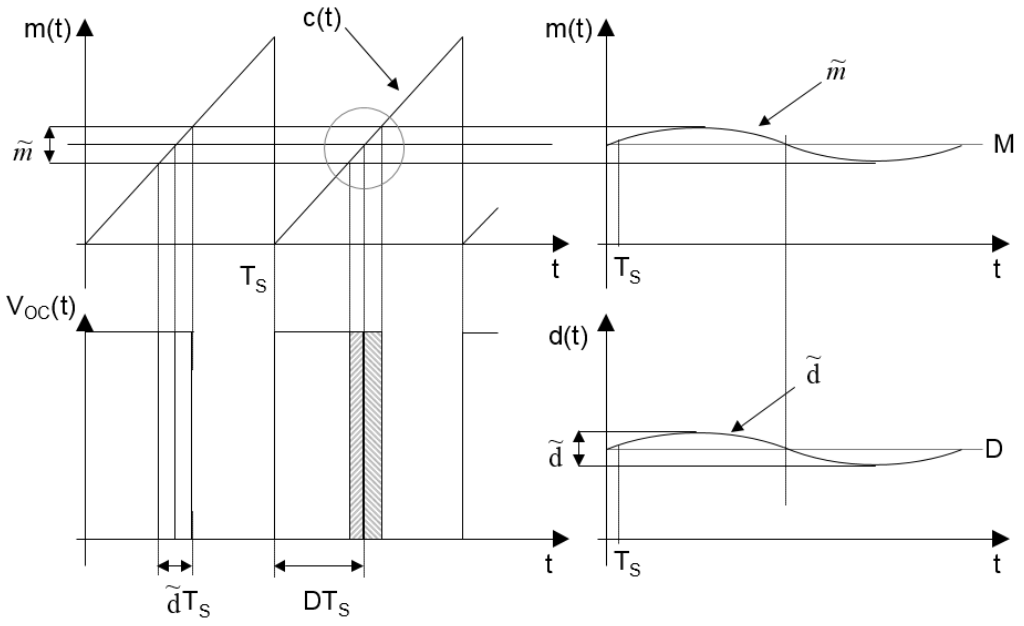

Fig. 3.3 Dynamic response of PWM modulator

3.1.2 Dead time in PWM modulator

In the synchronous DC-DC converter to avoid cross conduction dead time is required. A synchronous buck converter is shown in the Fig. 3.4. When the switch S_1 will go from ON to OFF, at the same time switch S_2 will go from OFF to ON. In this transition period both the switches will be in ON state and short circuit will occur.

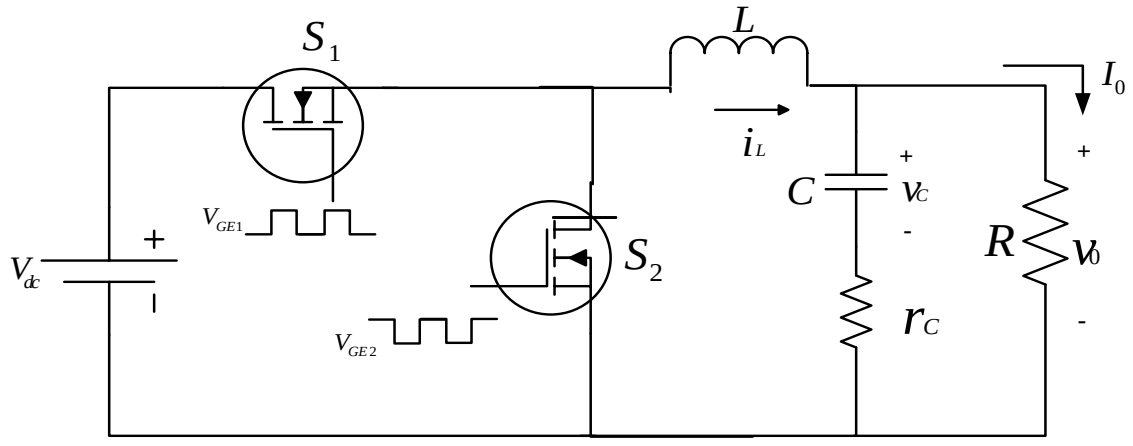

Fig. 3.4 Circuit diagram of synchronous buck converter

The representation of dead time of PWM signal is shown in Fig. 3.5. To avoid cross conduction, the modulator delays S_1 turn-on by a time t_{dead}, applying the V_{G1} and V_{G2} command signals to the switches. The duration of t_{dead} is long enough to allow the safe turn off of switch S_2

before switch S_1 is commanded to turn on, considering propagation delays through the driving circuitry, inherent switch turn off delays and suitable safety margins.

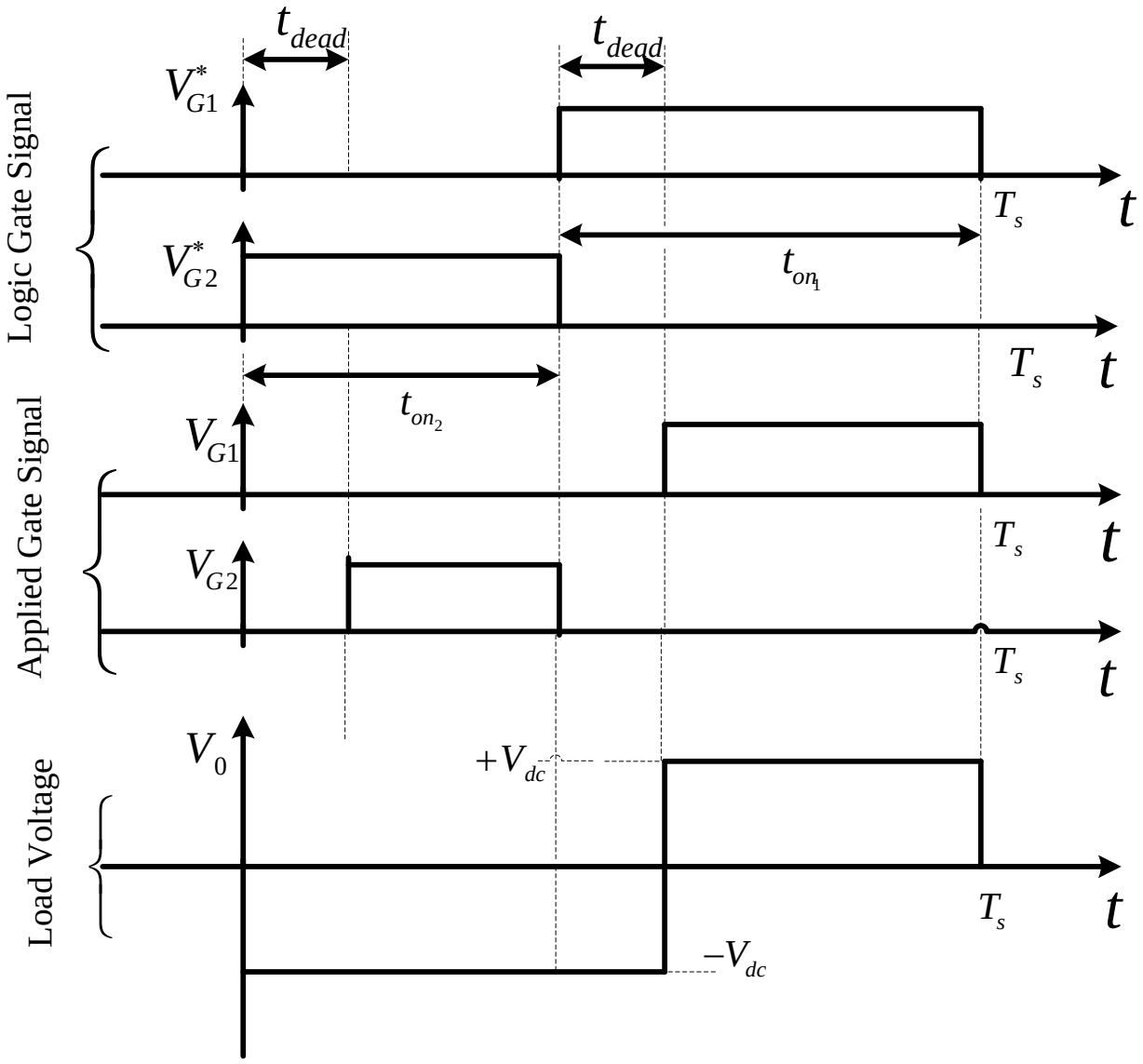

Fig. 3.5 Dead time representation of PWM signal

The effect of the dead time application is the creation of a time interval where both switches are in the off state. Because of that, an undesired difference is created between the duration of the S_1 switch on-time and the actual one that turns into an error in the voltage applied to the load. This error ΔV_0, whose entity is a direct function of dead time duration and whose polarity depends on the load current sign, according to the following relation:

$$\Delta V_0 = -2V_{DC}\frac{t_{dead}}{T_s} sign\left(I_0\right) \tag{3.6}$$

3.2 Digital Pulse Width Modulator

Digital pulse width modulator (DPWM) provides a digital to time domain conversion. In the DPWM first of all the time is quantized into discrete slots by using quantizer and then it is compared with digital input $d\left(n\right)$ in spite of a ramp signal. The block diagram of DPWM is shown in Fig. 3.6.

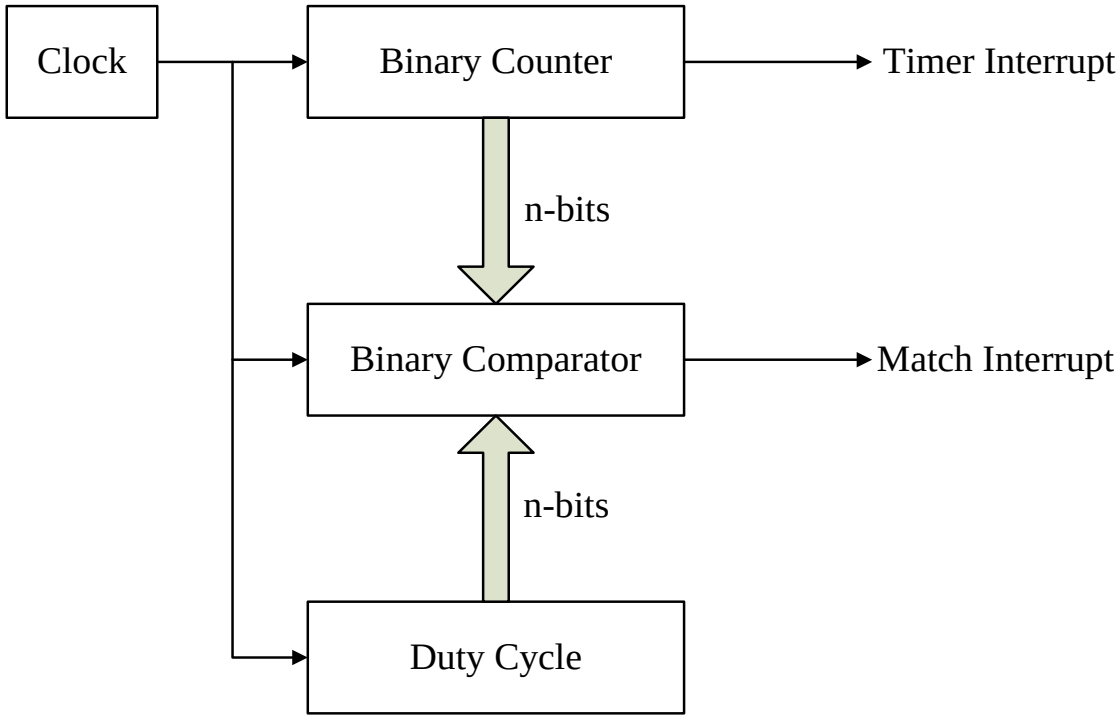

Fig. 3.6 Digital PWM modulator typical structure

As shown in the Fig. 3.6 the counter is incremented at every clock pulse; any time the binary counter value is equal to the programmed duty-cycle (match condition), the binary comparator triggers an interrupt to the microcontroller and at the same time sets the gate signal low. A typical analysis of the Fig. 3.6 is shown in graph below.

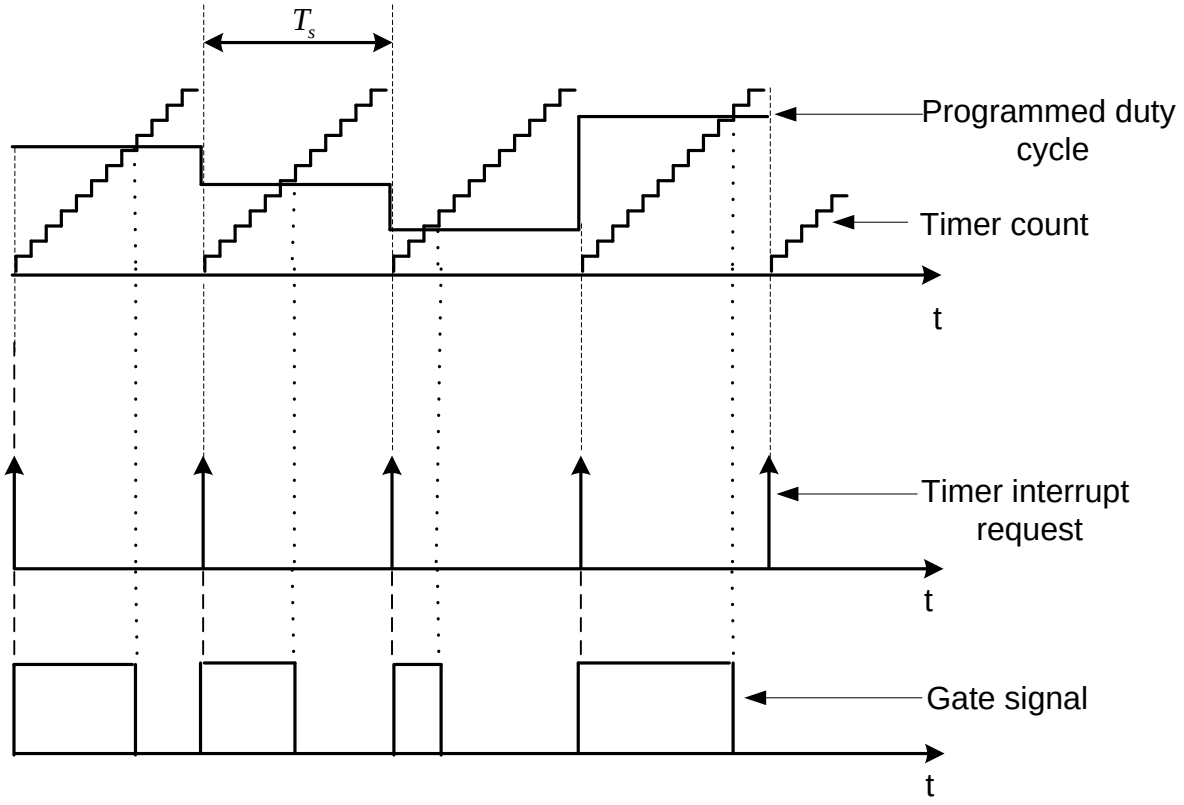

Fig. 3.7 Analysis plot of the digital PWM modulator

The gate signal is set high at the beginning of each counting (i.e. modulation) period, where another interrupt is typically generated for synchronization purposes. The counter and comparator have a given number of bits, n, which is often 16, but can be as low as 8, in the case a very simple microcontroller is used.

The dynamics of digitally controlled DC-DC converter are affected by two nonlinear effects: quantization effect and modulation effect. Due to the modulation effect there is a delay in the feedback loop. A uniformly sampled PWM is shown in Fig.3.8.

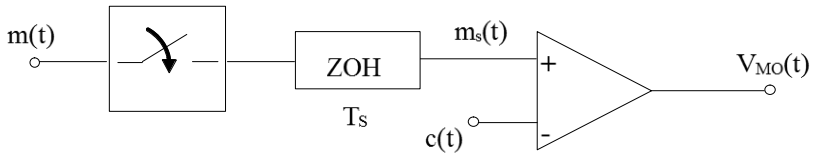

Fig. 3.8 A general uniformly sampled PWM

As shown in the above figure, the input signal $m(t)$ is sampled with a time period T_s and then the sampled input is hold with a zero order hold (ZOH) and then finally it is compared with

a triangular waveform $C(t)$ to generate the gate pulse of the MOSFET. Because of the sample and hold effect, the response of the modulator to any disturbance, e.g. to one requiring a rapid change in the programmed duty-cycle value, can take place only during the modulation period following the one where the disturbance actually takes place. This delay amounts to a dramatic difference with respect to the analog modulator implementation, where the response could take place already during the current modulation period, i.e. with negligible delay. The general perception of the dynamic behavior of the uniformly sampled PWM is improved by using Laplace domain and Z-domain models for uniformly sampled PWM [23].

3.2.1 Quantization and Limit Cycle

There is a limit cycle due to quantization effect of ADC and the DPWM in the digitally controlled DC-DC converter. Limit cycles refer to steady-state oscillations of output voltage V_{out} and other system variables at frequencies lower than the converter switching frequency f_{sw}. As shown in the Fig. 3.1 there are two quantizer in control loop of a digitally controlled DC-DC converter: one is in ADC and another in the DPWM. Let us assume that the resolution of the ADC is N_{adc} bit and the resolution of DPWM is N_{dpwm}. Then, for a buck converter the voltage quantization for ADC $\Delta V_{adc} = V_{in} / 2^{N_{adc}}$ and for the DPWM $\Delta V_{dpwm} = V_{in} / 2^{N_{dpwm}}$. The quantitative behavior of output voltage V_{out} in steady state is shown in Fig. 3.9 when ADC resolution is greater than DPWM resolution.

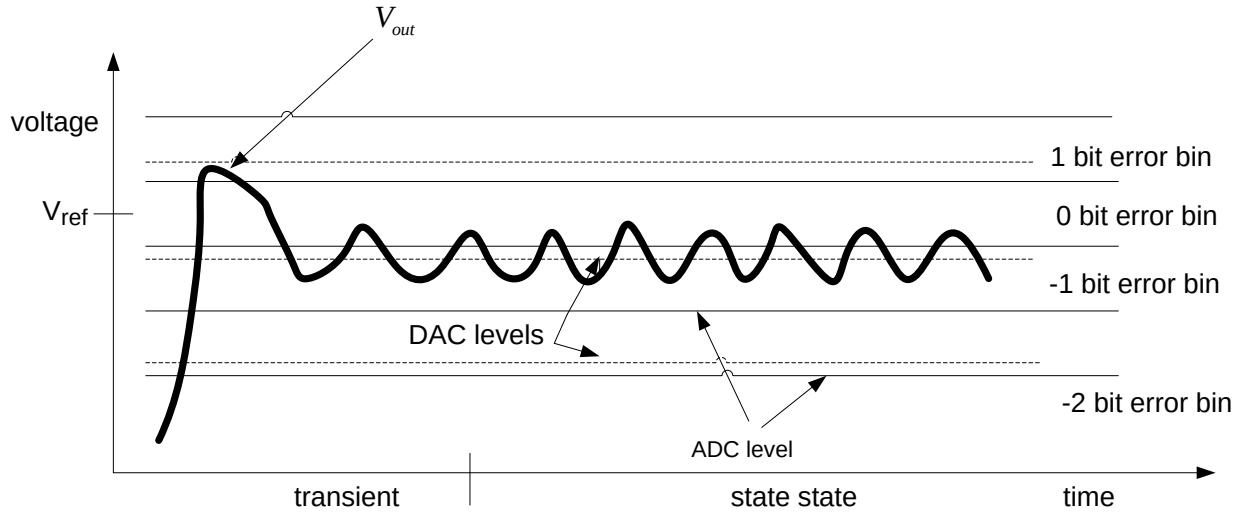

Fig. 3.9 Qualitative behaviour of V_{out} with ADC resolution greater than the DPWM resolution

As shown in the above figure, corresponding to reference voltage V_{ref}, no DPWM level maps into ADC bin. In the steady state, the control loop will try to drive output voltage V_{out} into zero error bin but due to no DPWM level in the zero error bin, it will alternate around zero error bin between the DPWM levels resulting into steady state limit cycle.

3.2.2 Elimination of Limit Cycle

To eliminate the limit cycle first of all there should be always a DPWM level that maps into zero error bin and this is possible only when the DPWM resolution is greater than the ADC resolution i.e. $N_{dpwm} > N_{adc}$. After meeting this condition, there can be still limit cycle if there is no integral term in the control law. In such case to drive output voltage V_{out} into zero error bin, the controller depends on the error signal. When the output voltage will reach in zero error bin, the error signal will become zero and V_{out} will drop again out of zero error bin. Repetition of this sequence will result in the steady state limit cycle. For solving this problem an integral term is necessary in the control law. So, the second limit cycle condition is $0 < K_i \leq 1$. The qualitative behavior of the output voltage V_{out} with DPWM resolution greater resolution and with an integral term included in control law is shown in Fig. 3.10.

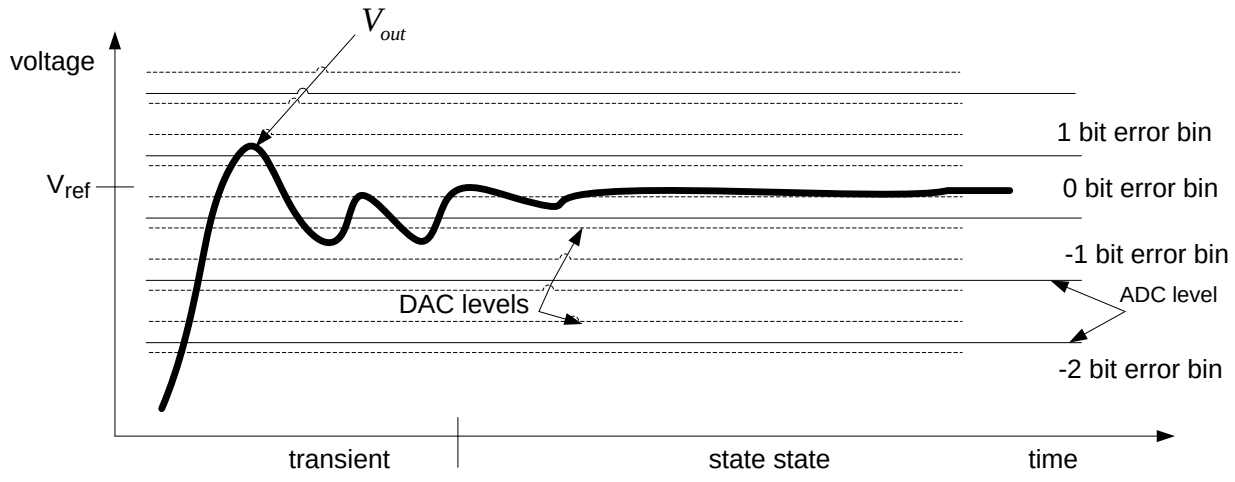

Fig. 3.10 Qualitative behaviour of V_{out} with DPWM resolution greater than ADC resolution and with integral term

As shown in the above figure after including the integral term in the controller, V_{out} reaches into zero error bin. After a transient, the integrator will gradually converges to a value that drives V_{out} into zero error bin.

3.3 Design of PID controller

In most of the cases the analog PID controllers are designed firstly and then it is converted into the equivalent discrete domain by using some transformation method like Backward Euler method, Bilinear method and pole-zero matching etc. Z-domain transfer function of the converter and modulator is needed for designing a digital controller directly. Small signal analysis of digitally controlled converters in z-domain is required to find the transfer function of converter and modulator in z-domain.

3.3.1 Root Locus Method

Root locus method is used to design the controller transfer function in a closed loop system. In the root locus method with the gain variation from zero to infinity, the closed loop poles of the system are plotted in the complex plane. By this method as the gain varies, the stability of the system and the pole location can be analyzed. In the root locus plot the pole radius from the origin corresponds to natural frequency and the imaginary part of the pole corresponds to damped natural frequency. The slowest response of the system determines the settling time of the system. The settling time of the system can be reduced by placing a pole for left in the left hand plane of the plot and the overshoot can be decreased by placing a real pole.

First of all the open loop transfer function of the system should be obtained to design the PID controller using root locus method. In the root locus plot if the locus of the system transfer function passes through right hand plane then the system is unstable and if the locus remains in the left hand plane then the system is stable. A system is considered as marginally stable when the root locus falls in the imaginary axis.

3.3.1.1 Procedure to Design PID Controller using Root Locus Method

The block diagram of a closed loop system is shown in Fig. 3.11. Where G_c is the transfer function of the PID controller, G_p is the plant transfer function and H is the feedback parameter.

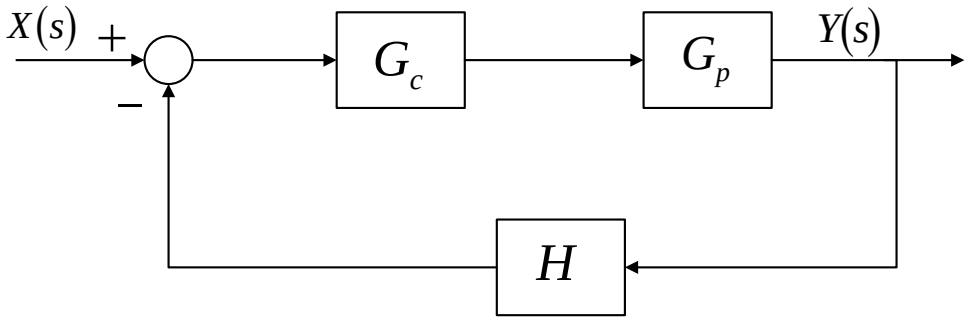

Fig. 3.11 Block diagram of a closed loop system

The procedure to design the PID controller is given below:

- On the basis of the requirement of the application define a set of transient specification.
- To meet these transient specification, find a pair closed loop poles s_1 and s_2.
- Find the steady state error e_{ss} of the system and define K_I for the defined e_{ss}.
- Lump integral term K_I/S into G_c together with plant transfer function G_p.
- Find K_p and K_d by using the equation given below:

$$G_p G_c(s_1) = -1 \tag{3.7}$$

or

$$K_p + K_d s_1 = -\frac{1}{G_c(s_1)} - \frac{K_I}{s_1} \tag{3.8}$$

- Find K_p and K_d by equating the real and imaginary part of eq. 3.8.

3.3.2 Frequency Response Method

Root locus method is also used to design the controller transfer function in a closed loop system. From frequency response method it is easy to design a compensator in spite of PID controller. In frequency response method magnitude and phase of the system is used to meet the design specification in spite of poles and zeros in root locus method. In the bode plot each term of PID controller is defined differently. The proportional term adjusts the gain margin and the phase margin of the system by changing the magnitude of the bode plot. A slope of -20dB/decade is added to the phase of the system by inclusion of integral term in the PID controller and it tends to unstabilize the system by changing the phase angle of the system with a constant -90 degree angle. The effect of the derivative term is just opposite of the integral term. A slope of +20dB/decade is

added to the phase of the system by inclusion of derivative term in the PID controller and it tends to unstabilize the system by changing the phase angle of the system with a constant +90 degree angle.

The phase margin and gain margin defines the stability of the system in the frequency response method. The phase cross over frequency is the frequency when the phase angle -180 degree and the gain magnitude below 0 dB at phase cross over frequency is the gain margin of the system. The gain cross over frequency is the frequency when the gain of the system is unity and the angle distance above -180 degree at gain cross over frequency is the phase margin of the system. If the magnitude plot is not reaching below 0 dB line at phase cross over frequency or if the phase of system is not above -180 degree at gain cross over frequency then the system is unstable.

3.3.2.1 Procedure to Design PID Controller using Frequency Response Method

- The open loop system should be stable to apply frequency response method.
- Draw the Bode plot of the open loop system.
- On the basis of the requirement of the application define a set phase margin, gain margin and crossover frequency of the system.
- From the mathematical analysis of the system, the phase margin of the system is depends on the damping ratio ξ of the system. The relation between phase margin and ξ is given below.

$$Phase\ M\arg in = \tan^{-1}\frac{2\xi}{\sqrt{-2\xi^2+\sqrt{1+4\xi^4}}} \tag{3.9}$$

- The crossover frequency ω_c and natural frequency ω_n are also related to damping ratio as given in the eq. 3.10.

$$\frac{\omega_c}{\omega_n} = \sqrt{-2\xi^2+\sqrt{1+4\xi^4}} \tag{3.10}$$

- On the basis of the design specification of the closed loop system, the K_p, K_I and K_d are designed so that phase margin and crossover frequency of the system can be fulfilled.

3.3.3 Ziegler-Nichols Tuning Method

Based on the transient response of the given system the values of proportional gain K_p, derivative time T_d and integral time T_i are determined using Zeigler-Nichols method. There are two methods for Zeigler-Nichols tuning, one is based on the step response and another is based on the critical period P_{cr} and critical gain K_{cr}. The Zeigler-Nichols tuned PID controller is represented as:

$$G_c(S) = K_p\left(1 + \frac{1}{T_i S} + T_d S\right) \tag{3.11}$$

3.3.3.1 Ziegler-Nichols Tuning Rule based on Step Response

- Find the unit step response of the system. The graph will look like S-shape as shown in Fig. 3.12.

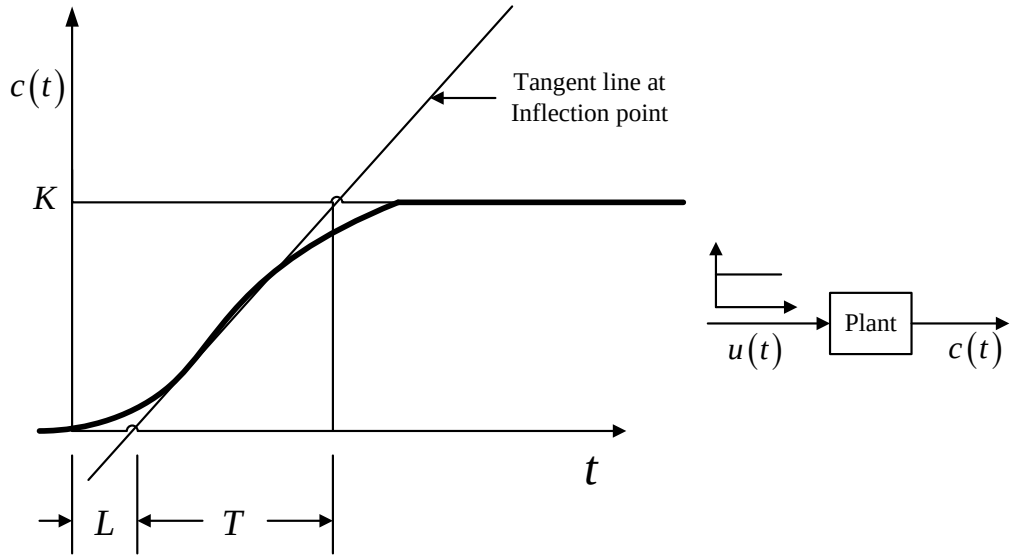

Fig. 3.12 Unit step Response of the open loop system

- Find delay time L and time constant T by drawing a tangent line as shown Fig. 3.12
- A first order system approximated transfer function with a transport delay is given as:

$$\frac{C(S)}{U(S)} = \frac{Ke^{-LS}}{TS+1} \tag{3.12}$$

- According to Ziegler and Nichols the values of K_p, T_i and T_d are given in the Table 3.1.

Table 3.1 Step Response based Ziegler-Nichols tuning of Controller

Type of Controller	P	PI	PID
K_p	T/L	$0.9T/L$	$1.2T/L$
T_i	∞	$L/0.3$	$2L$
T_d	0	0	$0.5L$

- Put the value of K_p, T_i and T_d from the Table 3.1 in eq. 3.11 to find the transfer function of the controller.

3.3.3.2 Ziegler-Nichols Tuning Rule based Critical Period and Critical Gain

- In this method first of all apply only proportional controller K_p in the closed loop unity feedback system as shown in the Fig. 3.13.

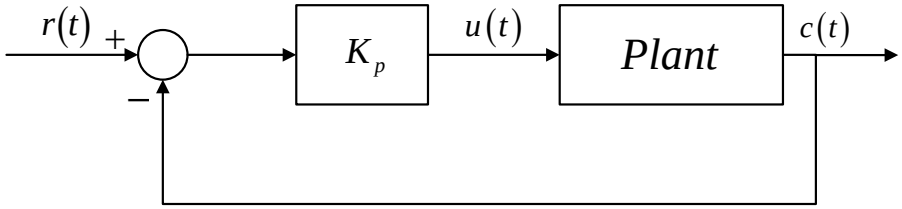

Fig. 3.13 Closed loop system with proportional controller

- Increase K_p from zero to a value where output exhibits oscillation, this value of K_p is called critical gain K_{cr} and the corresponding period is called critical period P_{cr} as shown in Fig. 3.14.

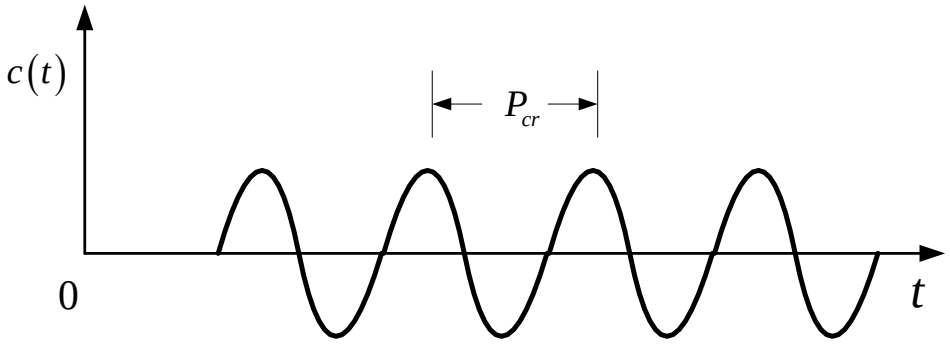

Fig. 3.14 Sustained oscillation with period P_{cr}

- According to Ziegler and Nichols the values of K_p, T_i and T_d are given in the Table 3.2.Table 3.2 Ziegler-Nichols tuning of Controller based on K_{cr} and P_{cr}

Type of Controller	P	PI	PID
K_p	$0.5K_{cr}$	$0.45K_{cr}$	$0.6K_{cr}$
T_i	∞	$P_{cr}/1.2$	$0.5P_{cr}$
T_d	0	0	$0.125P_{cr}$

- Put the value of K_p, T_i and T_d from the Table 3.2 in eq. 3.11 to find the transfer function of the controller.

3.3.4 Analog to digital PID

Laplace-domain transfer function of compensator is mapped into z-domain by approximation methods. The continuous Laplace-domain transfer function can be easily translated into discrete equivalent by using difference approximation, Backward Euler method, ZOH (zero-order hold), Bilinear method and pole-zero matching. The difference approximation equation is derived in this section. The approximation of the proportional term K_p of the PID controller is given below:

$$K_P e(n) \tag{3.13}$$

The integral term K_I of the PID controller using backward rectangular rule is approximated as:

$$K_I T e(n-1) \tag{3.14}$$

Also, the derivative term K_d of PID controller using backward difference is approximated as:

$$\frac{K_d}{T}\left[e(n)-e(n-1)\right] \tag{3.15}$$

Where, $e(n)$ is the error input to PID controller and T is the sample period.

From the above equations it can be seen that the integral term needed previous information. By adding the above three equations the complete structure of PID is defined as:

$$d(n) = K_P e(n) + \frac{K_d}{T}\left[e(n) - e(n-1)\right] + a(n) \tag{3.16}$$

$$a(n) = a(n-1) + K_I T e(n-1) \tag{3.17}$$

The above equation defines the position algorithm depends on the present control output and the velocity algorithm for the PID controller is given as:

$$d(n-1) = K_P e(n-1) + \frac{K_d}{T}\left[e(n-1) - e(n-2)\right] + a(n-1) \tag{3.18}$$

$$a(n-1) = a(n-1) + K_I T e(n-2) \tag{3.19}$$

By subtracting Eq. (3.18) from Eq. (3.16), the approximation of digital PID controller is given as:

$$d(n) - d(n-1) = K_P\left[e(n) - e(n-1)\right] + \frac{K_d}{T}\left[e(n) + e(n-2) - 2e(n-1)\right] + K_I T e(n-1) \tag{3.20}$$

CHAPTER 4

Voltage Mode Control

4.1 Voltage Mode controlled Buck Converter

In the voltage mode control the output voltage of the DC-DC converter is used as feedback signal. The error input to the PID controller is generated by comparing the output voltage v_0 with the desired output v_{ref}. The controller generates the control signal in accordance with the error signal. The voltage mode controlled Buck converter is shown in Fig. 4.1.

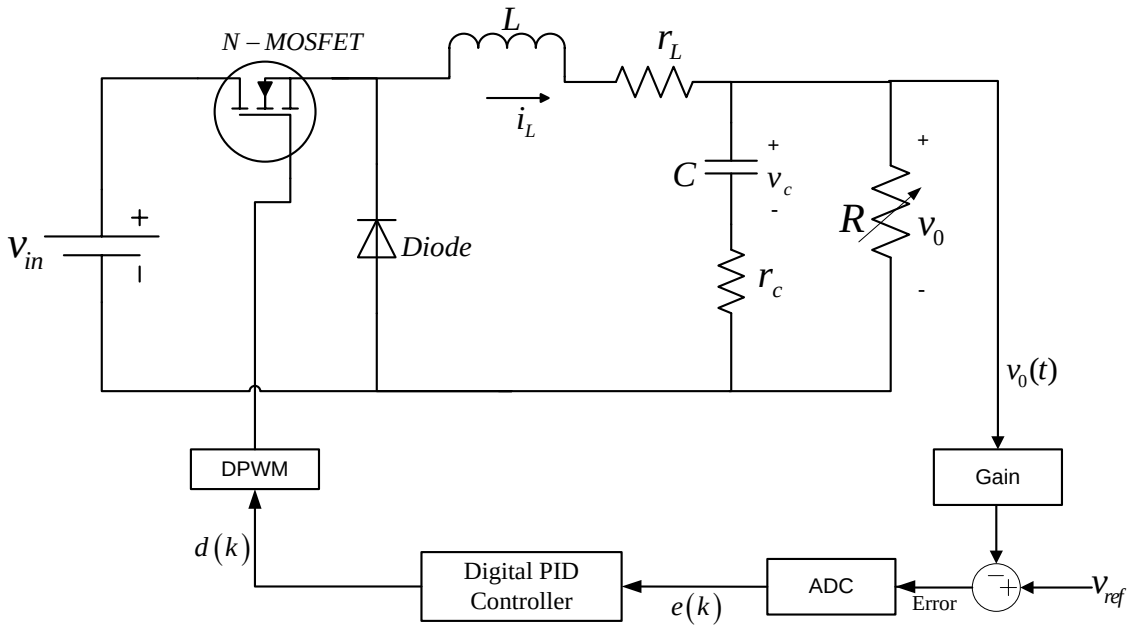

Fig. 4.1 Voltage mode controlled Buck converter

As shown in the above figure the output voltage is used for feedback signal. The proposed voltage mode controlled Buck converter is tasted for input voltage $v_{in} = 6V$, switching frequency $f_s = 100\,k\text{Hz}$, inductance $L = 22.5\,mH$, ESR of inductor $r_L = 20\,m\Omega$, capacitance $C = 12.5\,\mu F$, and ESR of capacitor $r_C = 3\,m\Omega$. By using Eq. (2.39) the transfer function of the buck converter is defined as:

$$G_{v_0 d}(s) = \frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{4.5\times10^{-6}s + 120}{2.81\times10^{-8}s^2 + 2.28\times10^{-4}s + 10} \tag{4.1}$$

By using Ziegler-Nicholas step response method the following PID controller is obtained:

$$G_c(s) = 0.2002 + \frac{4004.7}{s} + 2.5\times10^{-4}s \tag{4.2}$$

By using Bilinear Transformation i.e. $S = \frac{2}{T_s}\frac{(Z-1)}{(Z+1)}$ Eq. (4.2) is transformed into discrete form, which is given below:

$$G_c(\mathrm{Z}) = \frac{50.22Z^2 - 99.96Z + 49.82}{Z^2 - 1} \tag{4.3}$$

4.1.1 Simulation Result

Step response of the above system is given in Fig. (4.2). The settling time, peak over shoot and the rise time of the open loop system is greater than the close loop system.

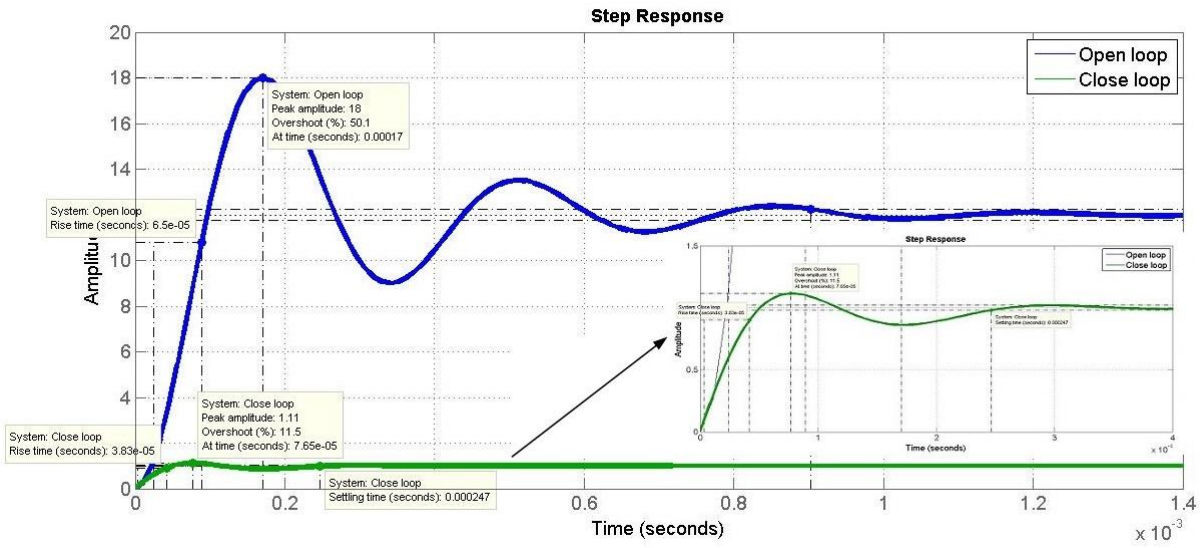

Fig. 4.2 Step response of the open loop and closed loop system

From the step response of the system it is clear that the closed loop system with PID controller is more stable than the open loop system and the transient response of the closed loop system is also better than the open loop system. Bode plot of the system is given in Fig. (4.3).

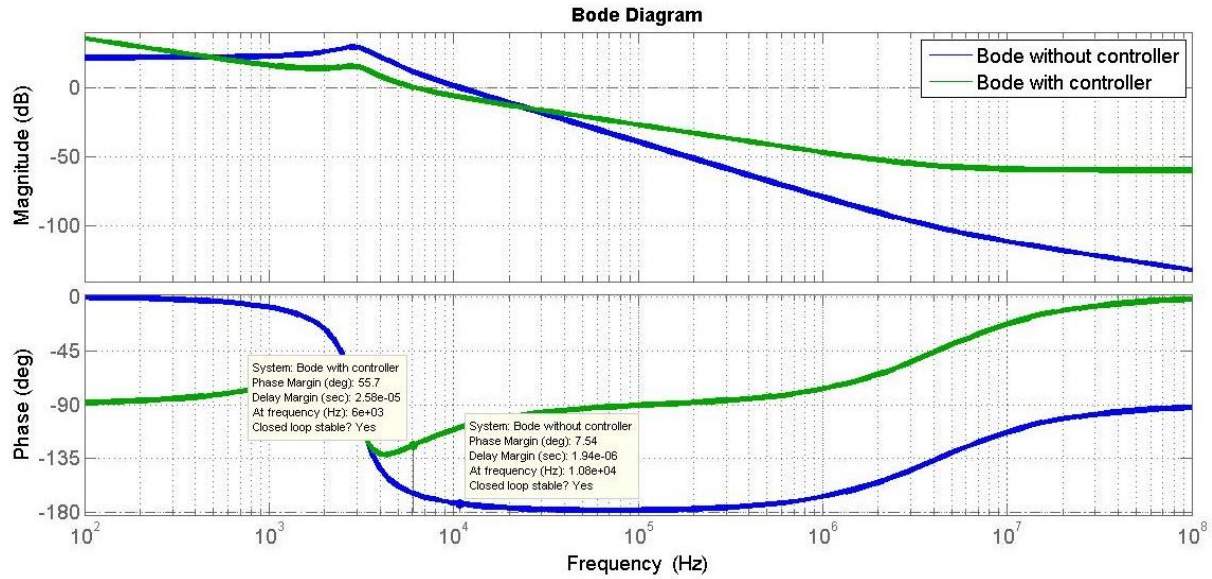

Fig. 4.3 Bode plot of the system

From the bode plot in the above figure it can be seen that the phase margin of the system with PID controller is greater than the system alone. That means the stability of the system is increased with inclusion of PID controller.

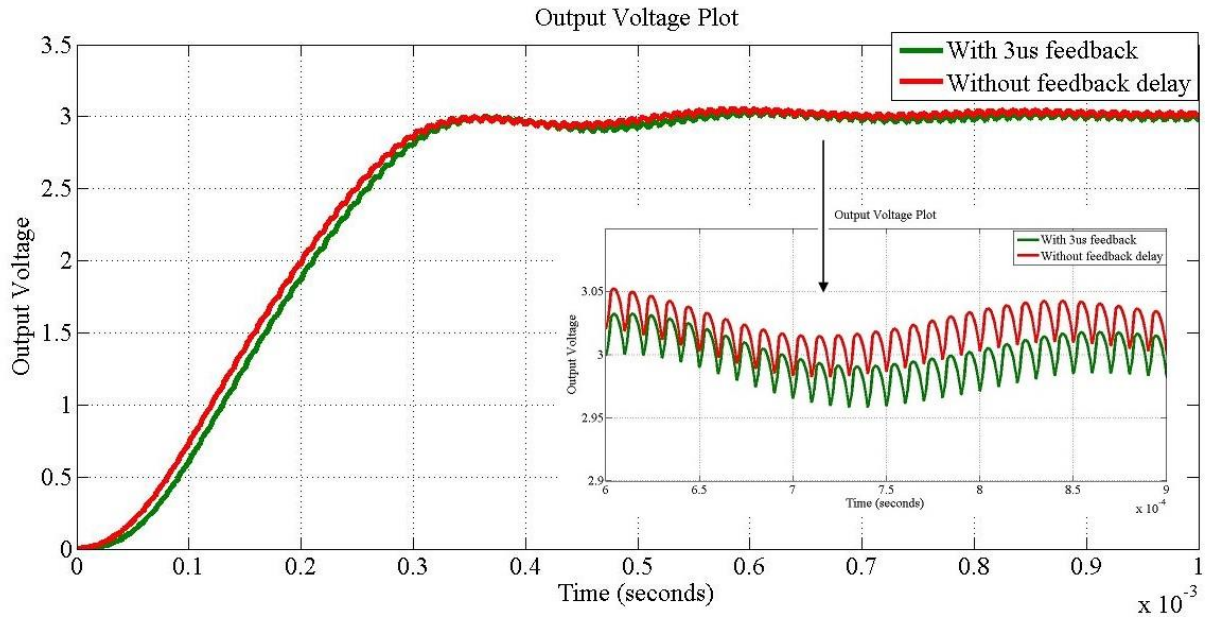

Fig. 4.4 Simulation output voltage of buck converter with constant load

The simulation output of the buck converter is shown in the Fig. (4.4). The system with feedback delay is lagging behind the system without feedback delay.

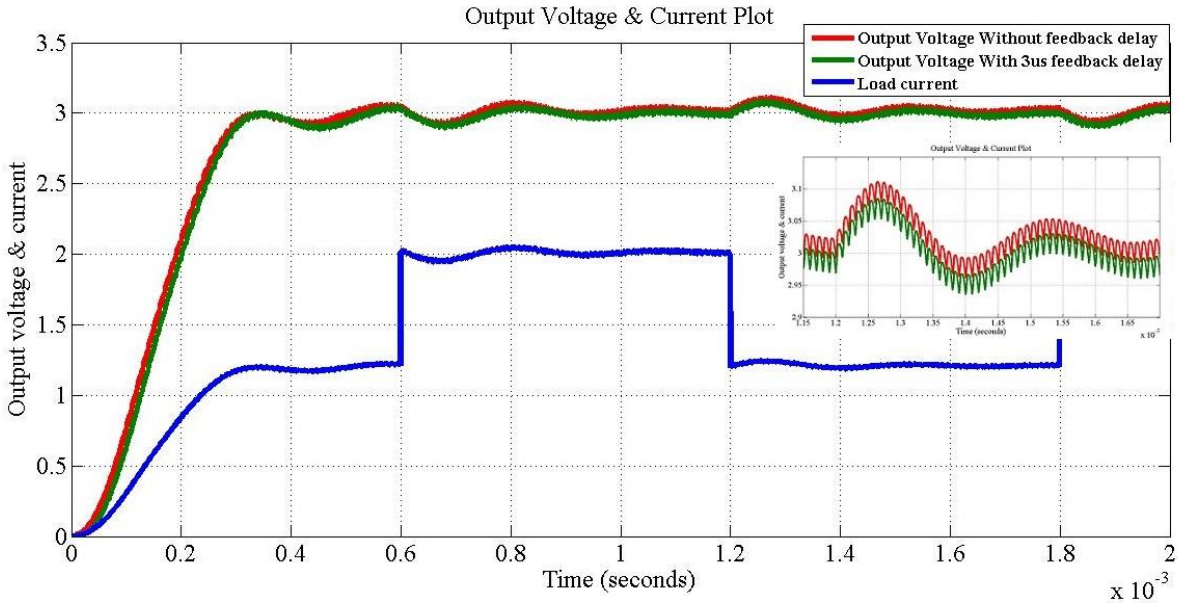

Fig. 4.5 Simulation output voltage of buck converter with small load variation

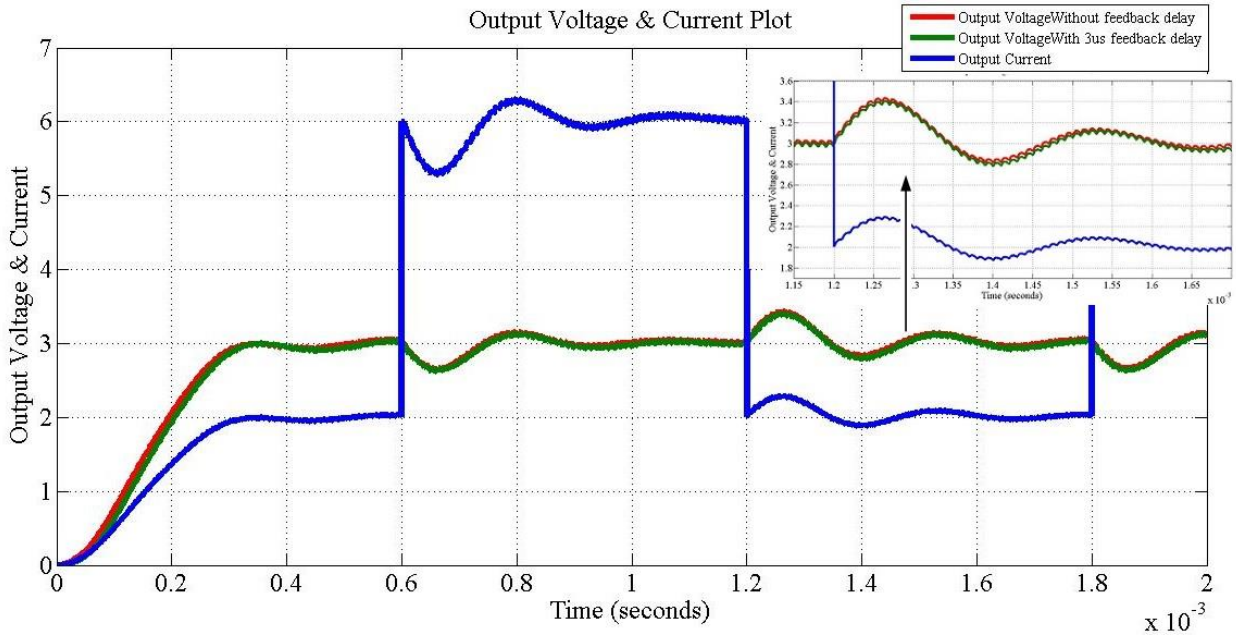

Fig. 4.6 Simulation output of buck converter with large load variation

The simulation output of the buck converter is shown in the Fig. (4.5) and (4.6). The peak overshoot of the system with large load variation is larger than the peak overshoot of the system having small load variation. The settling time of both of the system is same.

4.1.2 Hardware Result

The hardware setup for voltage mode control is given in Fig.4.7. The PWM signal and corresponding output voltages are given below.

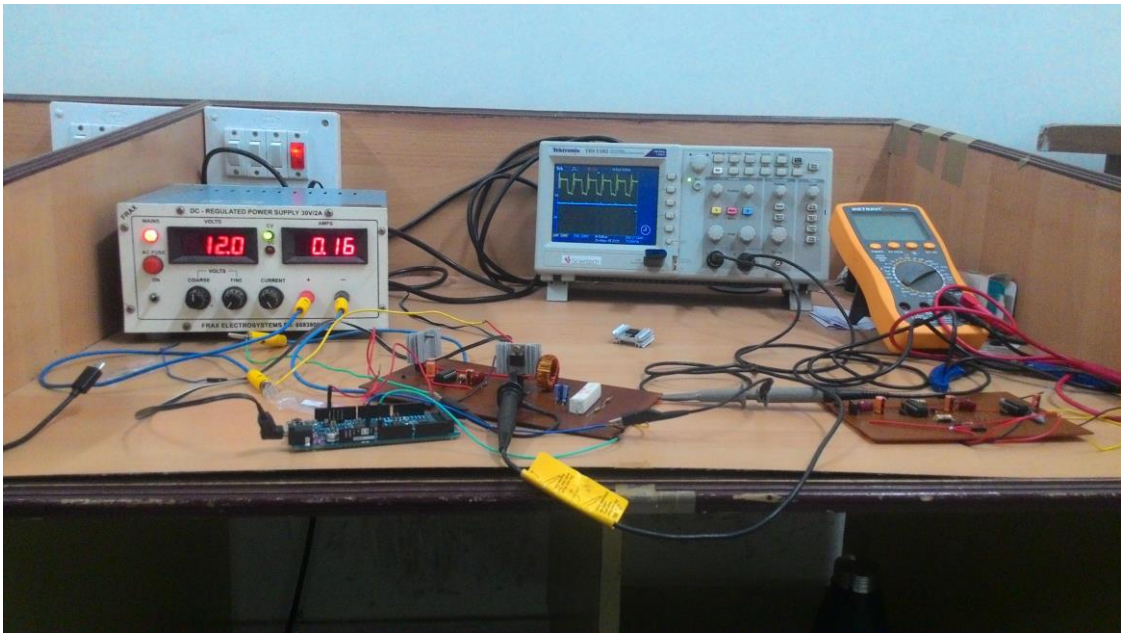

Fig. 4.7 Hardware setup for voltage mode control

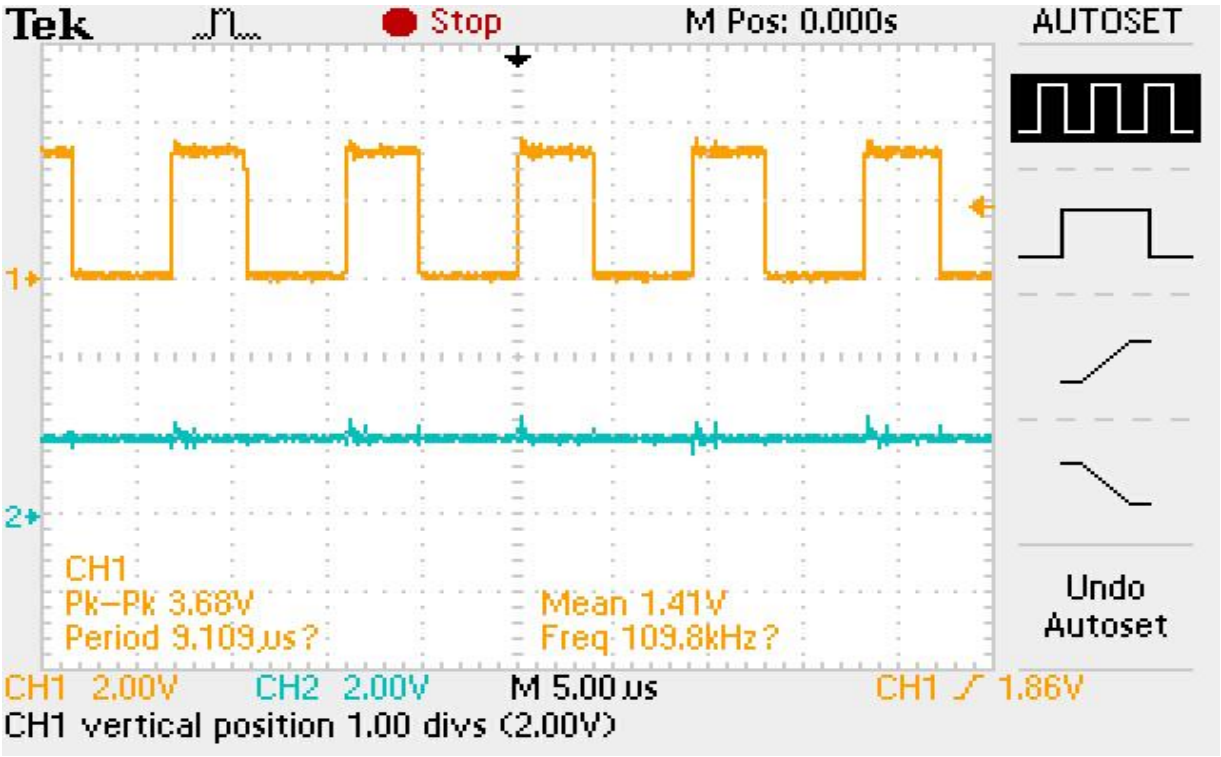

Fig. 4.8 Output voltage and PWM signal with 2V reference signal

The PWM signal and the output voltage is shown in Fig. 4.8. Channel 1 (CH1) of the CRO is showing the PWM signal and channel 2 (CH2) is showing the output voltage. The output voltage is following the reference signal in steady state.

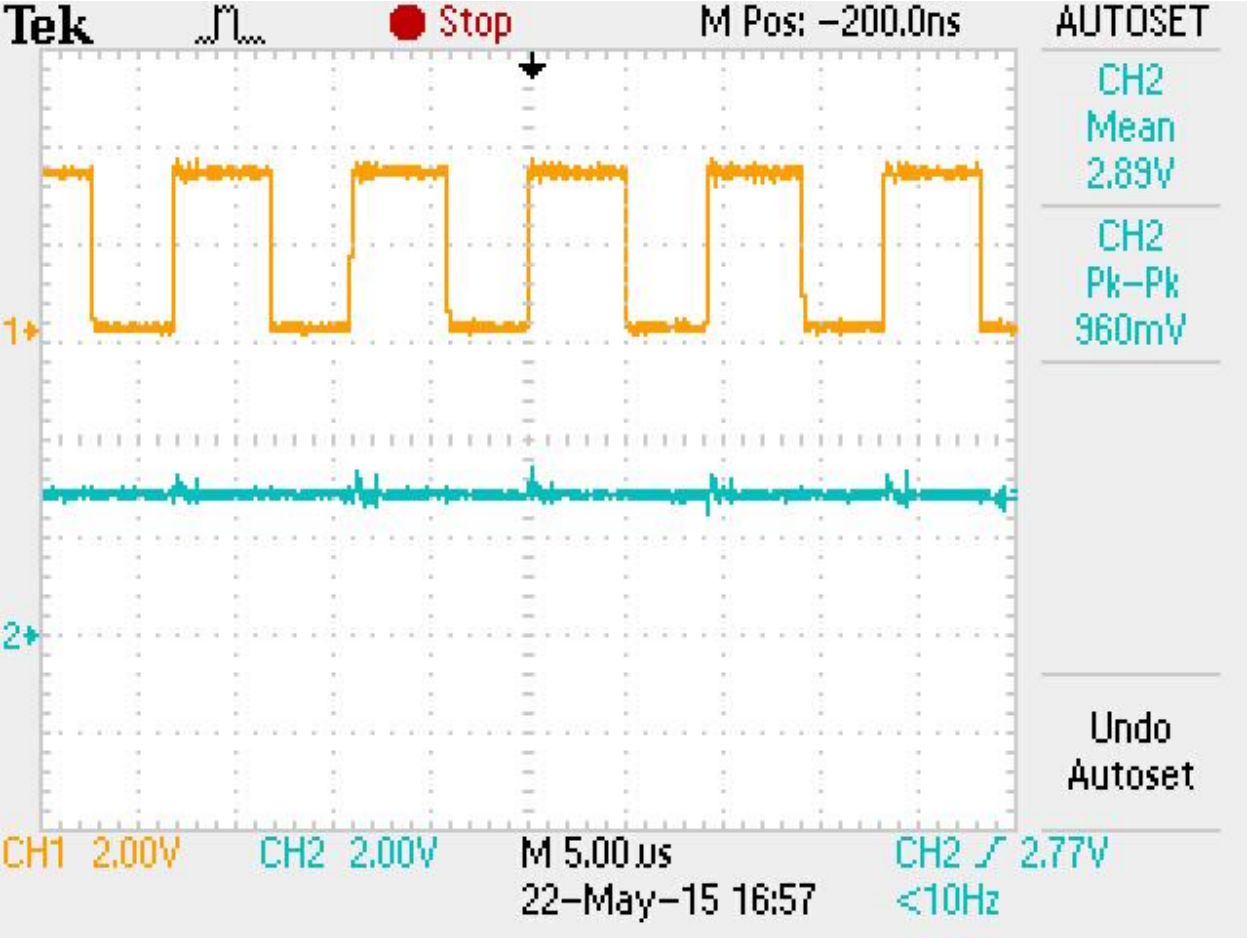

Fig. 4.9 Output voltage and PWM signal with 3V reference signal

The above figure shows the output voltage and the PWM signal with 3V reference signal. From the above two output is can be observed that the output voltage and PWM duty cycle is synchronized and in accordance with the reference signal. The AC coupled output voltage is shown in Fig. 4.10.

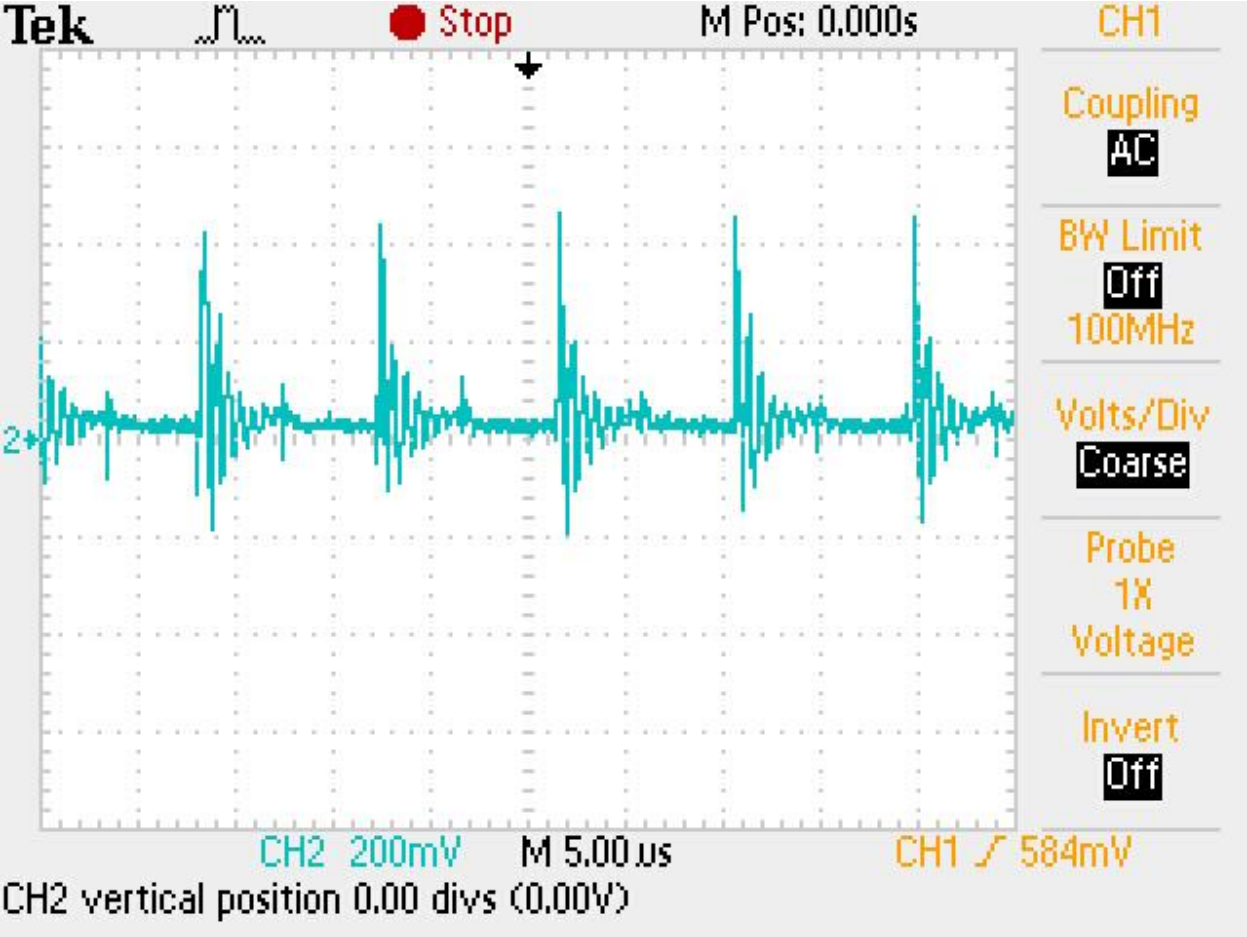

Fig. 4.10 AC coupled output voltage

4.2 Voltage Mode controlled Boost Converter

In the voltage mode control the output voltage of the DC-DC converter is used as feedback signal. The error input to the PID controller is generated by comparing the output voltage v_0 with the desired output v_{ref}. The controller generates the control signal in accordance with the error signal. The voltage mode controlled Boot converter is shown in Fig. 4.12.

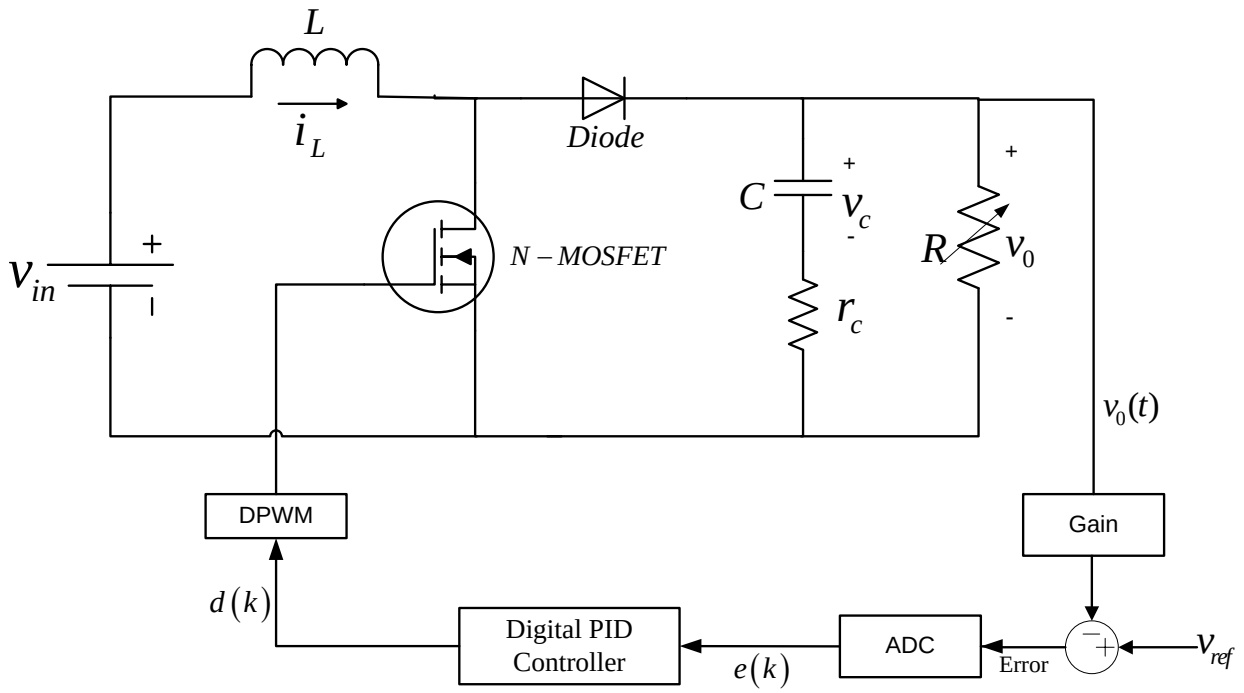

Fig. 4.12 Voltage mode controlled Boost converter

As shown in the above figure the output voltage is used for feedback signal. The proposed voltage mode controlled Buck converter is tasted for input voltage $v_{in} = 5V$, switching frequency $f_s = 100\,k\text{Hz}$, inductance $L = 80\,\mu H$, capacitance $C = 1.68\,\mu F$, and ESR of capacitor $r_C = 5\,m\Omega$. By using Eq. (2.39) the transfer function of the buck converter is defined as:

$$G_{v_0 d}(s) = \frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{-4.398\times10^{-12}s^2 - 5.225\times10^{-4}s + 120}{1.152s^2 + 11.582s + 2.2\times10^3} \tag{4.4}$$

By using Ziegler-Nicholas step response method the following controller is obtained:

$$G_c(s) = \frac{6.2583\times10^{-3}s^2 + 0.30339s + 1.3605}{8.1\times10^{-4}s^2 + s} \tag{4.5}$$

By using Bilinear Transformation i.e. $S = \frac{2}{T_s}\frac{(Z-1)}{(Z+1)}$ Eq. (4.5) is transformed into discrete form, which is given below:

$$G_c(z) = \frac{7.681Z^2 - 15.36Z + 7.677}{Z^2 - 1.988Z + 0.9877} \tag{4.6}$$

4.2.1 Simulation Result

The output voltage and the load current of the boost converter is given below. The settling time of the output voltage is $12msec$. From the results it can be observed that the load current and output voltage is synchronized.

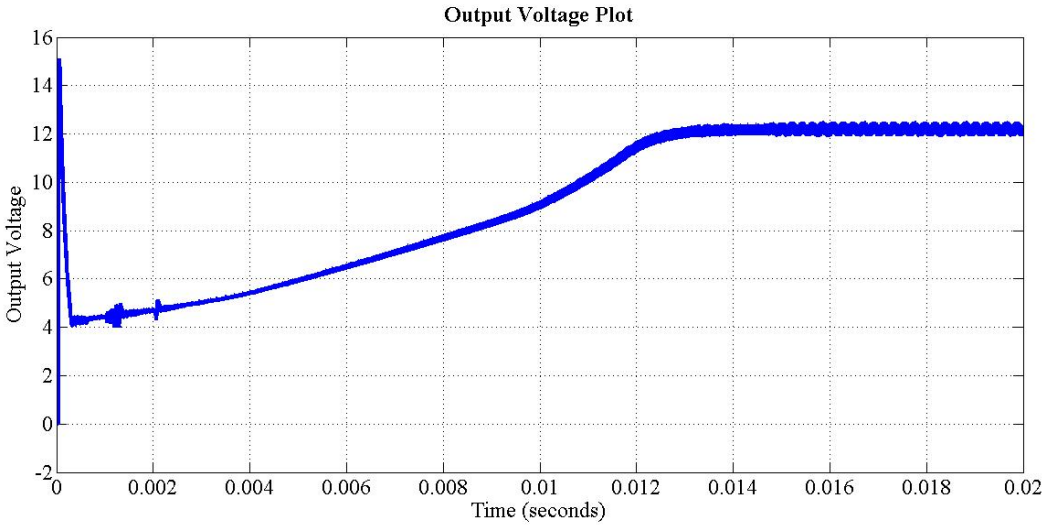

Fig. 4.11 Output voltage of boost converter

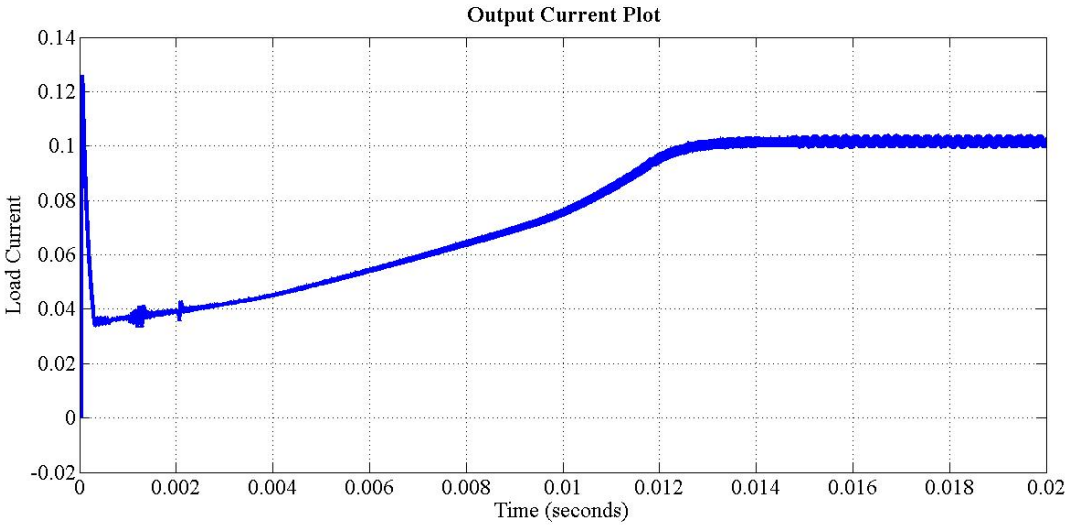

Fig. 4.12 Load current of the boost converter

CHAPTER 5

Current Mode Control

The current mode control is based on the inductor current. In the current mode control the transient response of the system is faster because of two control loops. The reference current is generated by additional loop and is used in the current control loop as the reference signal. The inductor current is forced to follow the reference current in the current mode control and the reference current is generated by the outer loop.

5.1 Current Mode Control for Buck Converter without Slope Compensation

In the current mode control without slope compensation the desired inductor current is forced in the next switching cycle to find the desired output voltage quickly. In this method input voltage V_{in}, output voltage V_0 and inductor current i_L is used in the control loop. The control signal generated by the outer loop is used as the reference current and is fed to the inner loop. The control signal generated by the inner loop contains two parallel terms and one of which vanishes when present inductor current follows previous reference current i.e. steady state.

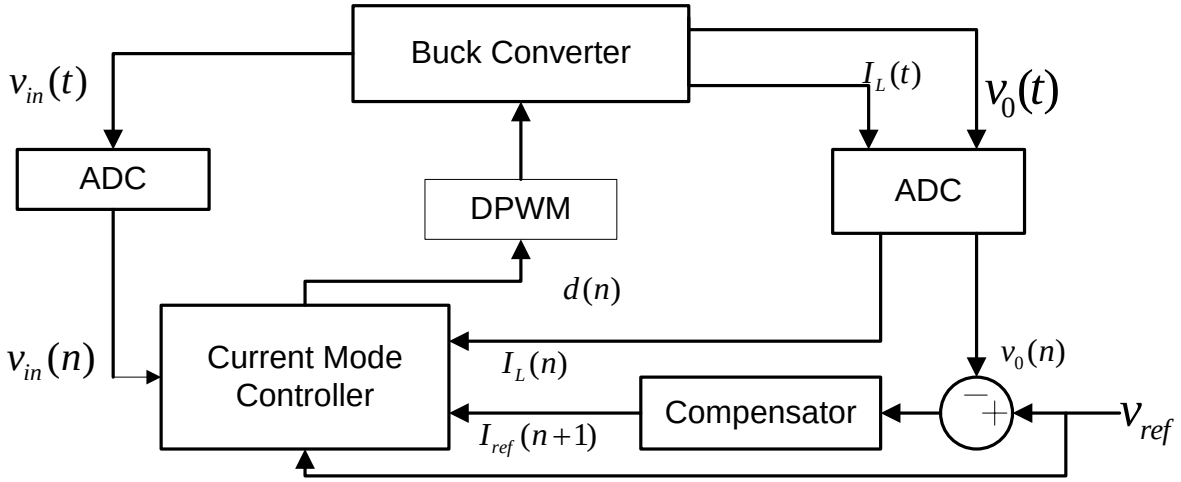

Fig. 5.1 Block diagram of current mode control without slope compensation

5.1.1 Principle of Current Control Law

As shown in the Fig. 4.1 the feedback control loop consists of several ADC, a DPWM, a compensator to control the reference current and a programmable current mode controller. By using Eq. (2.4) the inductor current of buck converter during ON time is defined as:

$$\frac{dI_L(t)}{dt} = \frac{1}{L}\left(v_{in}(t) - v_0(t)\right) \qquad for \qquad t(n) \le t < t(n) + d(n)T_s \tag{5.1}$$

During OFF time the inductor current is given as:

$$\frac{dI_L(t)}{dt} = \frac{1}{L}\left(-v_0(t)\right) \qquad for \qquad t(n) + d(n)T_s \le t < t(n+1) \tag{5.2}$$

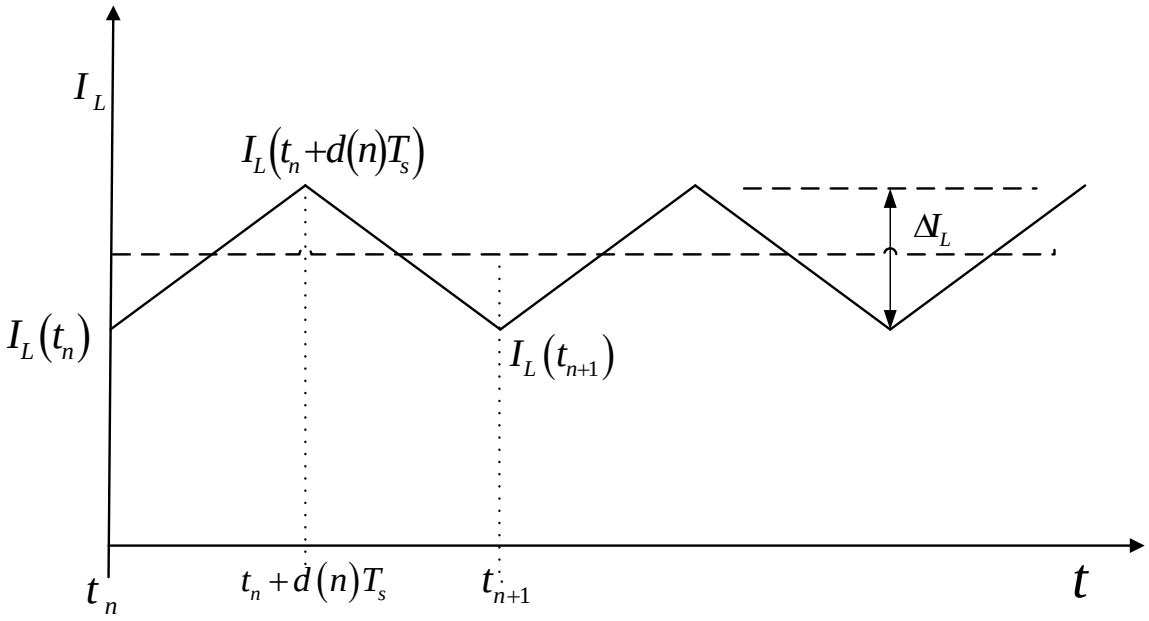

Fig. 5.2 Steady state inductor current

If the switching frequency of the converter is very high then the change in the inductor current over a very small time can be considered as:

$$\frac{dI_L(t)}{dt} \approx \frac{I_L(t + \Delta t) - I_L(t)}{\Delta t} \tag{5.3}$$

On substituting the value of Eq. (5.3) in Eq. (5.1) and (5.2):

$$\frac{I_L\left(t_n + d\left(n\right)T_s\right) - I_L\left(t_n\right)}{d\left(n\right)T_s} = \frac{1}{L}\left(v_{in}\left(t_n\right) - v_0\left(t\right)\right) \tag{5.4}$$

$$\frac{I_L\left(t_{n+1}\right) - I_L\left(t_n + d\left(n\right)T_s\right)}{\left(1 - d\left(n\right)\right)T_s} = \frac{1}{L}\left(-v_0\left(t_n\right)\right) \tag{5.5}$$

On simplifying Eq. (5.4):

$$I_L\left(t_n + d\left(n\right)T_s\right) - I_L\left(t_n\right) = \frac{\left(v_{in}\left(t_n\right) - v_0\left(t_n\right)\right)d\left(n\right)T_s}{L} \tag{5.6}$$

On substituting the value of $I_L\left(t_n + d\left(n\right)T_s\right)$ from Eq. (5.6) to Eq. (5.5):

$$I_L\left(t_{n+1}\right) - I_L\left(t_n\right) = -\frac{v_0\left(t_n\right)T_s}{L} + \frac{v_{in}\left(t_n\right)d\left(n\right)T_s}{L} \tag{5.7}$$

On simplifying Eq. (5.7) to find $d\left(n\right)$:

$$d\left(t_n\right) = \frac{L}{T_s}\frac{\left(I_L\left(t_{n+1}\right) - I_L\left(t_n\right)\right)}{v_{in}\left(t_n\right)} + \frac{v_0\left(t_n\right)}{v_{in}\left(t_n\right)} \tag{5.8}$$

To simplifying the Eq. (5.8), the following discrete form is proposed:

$$d\left(n\right) = \frac{L}{T_s}\frac{\left(I_L\left(n+1\right) - I_L\left(n\right)\right)}{v_{in}\left(n\right)} + \frac{v_0\left(n\right)}{v_{in}\left(n\right)} \tag{5.9}$$

The following discrete form of the Eq. (5.9) is proposed:

$$d\left(n\right) = \frac{L}{T_s}\frac{\left(I_L\left(n+1\right) - I_L\left(n\right)\right)}{v_{in}\left(n\right)} + \frac{v_0\left(n\right)}{v_{in}\left(n\right)} \tag{5.10}$$

In the steady state $I_L\left(n+1\right)$ should follow reference current $I_L\left(n+1\right)$ and output voltage $v_0\left(n\right)$ should follow reference voltage v_{ref}. Hence Eq. (5.10) can be expressed as:

$$d\left(n\right) = \frac{L}{T_s}\frac{\left(I_{ref}\left(n+1\right) - I_L\left(n\right)\right)}{v_{in}\left(n\right)} + \frac{v_{ref}\left(n\right)}{v_{in}\left(n\right)} \tag{5.11}$$

$$d\left(n\right) = d_1\left(n\right) + d_2\left(n\right) \tag{5.12}$$

Where,

$$d_1(n)=\frac{L}{T_s}\frac{\left(I_{ref}(n+1)-I_L(n)\right)}{v_{in}(n)} \quad and \quad d_2(n)=\frac{v_{ref}(n)}{v_{in}(n)} \tag{5.13}$$

Similarly, the current control law for Boost and Buck-Boost converter is derived by changing the second term $d_2(n)$ by their steady state duty ratio and is given below in Eq. (5.14) and (5.15) respectively.

$$d(n)=\frac{L}{T_s}\frac{\left(I_{ref}(n+1)-I_L(n)\right)}{v_{in}(n)}+\left(1-\frac{v_{ref}(n)}{v_{in}(n)}\right) \tag{5.14}$$

$$d(n)=\frac{L}{T_s}\frac{\left(I_{ref}(n+1)-I_L(n)\right)}{v_{in}(n)+v_{ref}(n)}+\frac{v_{ref}(n)}{v_{in}(n)+v_{ref}(n)} \tag{5.15}$$

For designing compensator transfer function output voltage v_0 to I_{ref} transfer function is required. The current loop expression given below is obtained ignoring the feed forward term.

$$\frac{v_0}{I_{ref}}=\frac{F_m G_{vd}(S)}{1+F_m G_{id}(S)} \tag{5.16}$$

From Eq. (2.39) and (2.42):

$$G_{vd}(s)=\frac{\hat{v}_0(s)}{\hat{d}(s)}=\frac{v_{in}R(1+sr_cC)}{s^2(R+r_c)LC+s(L+r_cRC)+R} \tag{5.17}$$

$$G_{Id}(s)=\frac{\hat{I}_L(s)}{\hat{d}(s)}=\frac{v_{in}(1+s(R+r_c)C)}{s^2(R+r_c)LC+s(L+r_cRC)+R} \tag{5.18}$$

5.1.2 Result and Discussion

The proposed method is tested on Buck converter having input voltage $v_{in}=5V$, switching frequency 400 kHz, inductance $L=0.33\mu H$, and capacitance $C=220\mu F$. By substituting these values in Eq. (5.17) and (5.18) the following transfer function obtained:

$$G_{vd}=\frac{3.125}{72.6\times10^{-12}S^2+0.33\times10^{-6}S+0.625} \tag{5.19}$$

$$G_{Id} = \frac{8.125}{72.6\times10^{-12}S^2 + 0.33\times10^{-6}S + 0.625} \tag{5.20}$$

On substituting Eq. (5.19) and (5.20) in (5.16) and assuming $F_m = 1$ the following transfer function is obtained:

$$\frac{V_0}{I_{ref}} = \frac{3.125}{72.6\times10^{-12}S^2 + 0.33\times10^{-6}S + 0.625} \tag{5.21}$$

Compensator for above transfer function having 60 kHz bandwidth and 58° phase margin of the closed loop system is given below.

$$G_c(S) = \frac{8.62\times10^{-6}S^2 + 1.53S + 6.03\times10^4}{S} \tag{5.22}$$

By using Bilinear Transformation i.e. $S = \frac{2}{T_s}\frac{(Z-1)}{(Z+1)}$ Eq. (5.22) is transformed into discrete form, which is given below:

$$G_C(Z) = \frac{3.615Z^2 - 2.965Z + 0.555}{Z^2 - 1} \tag{5.23}$$

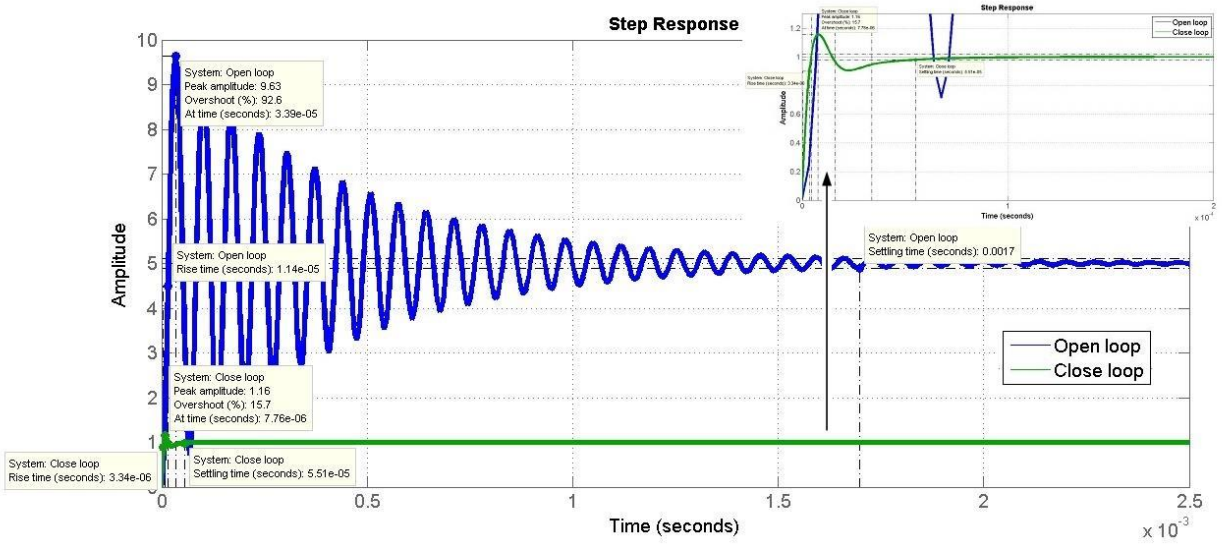

Fig. 5.3 Step Response of the open loop and closed loop system

The step response of the open loop and closed loop system is shown in the Fig. 5.3. From the figure it can be seen that the open loop step response is oscillatory while the close loop response

is stable with very small maximum overshoot, settling time and rise time as compared to the open loop system.

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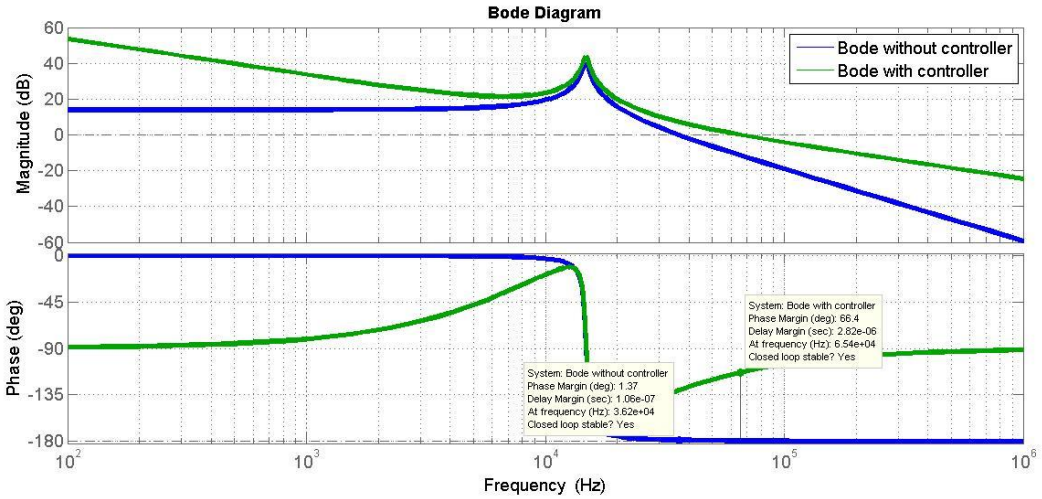

Fig. 5.4 Bode Plot of the system

The bode plot of the system without controller and with controller is shown in the Fig. 5.4. The phase margin of the system with controller is 66^0 while the phase margin of the system without controller is 1.5^0. That means the system with controller is more stable. The output voltage and the inductor current response of the simulation is shown in Fig. 5.5 and 5.6.

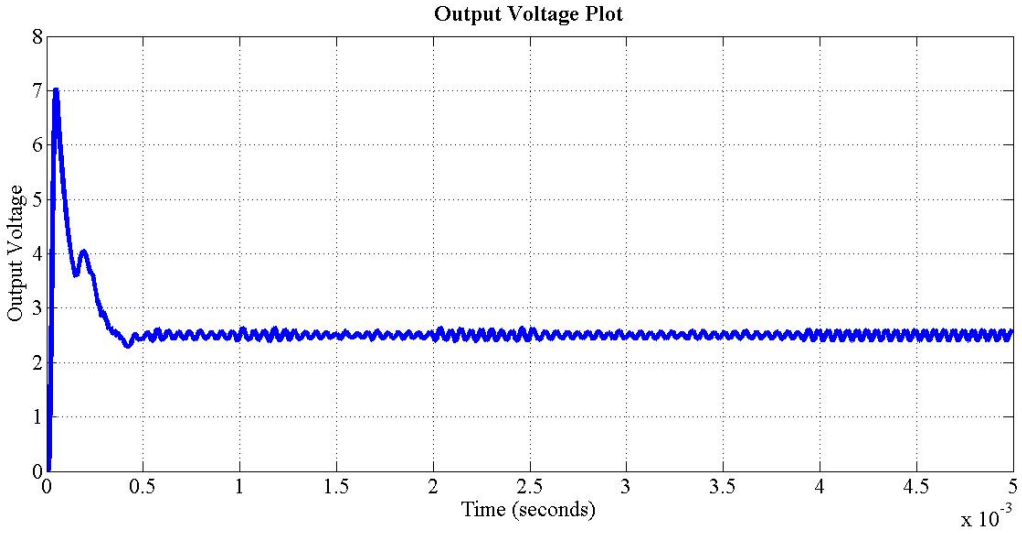

Fig. 5.5 Output Voltage Response of current mode controlled Buck converter

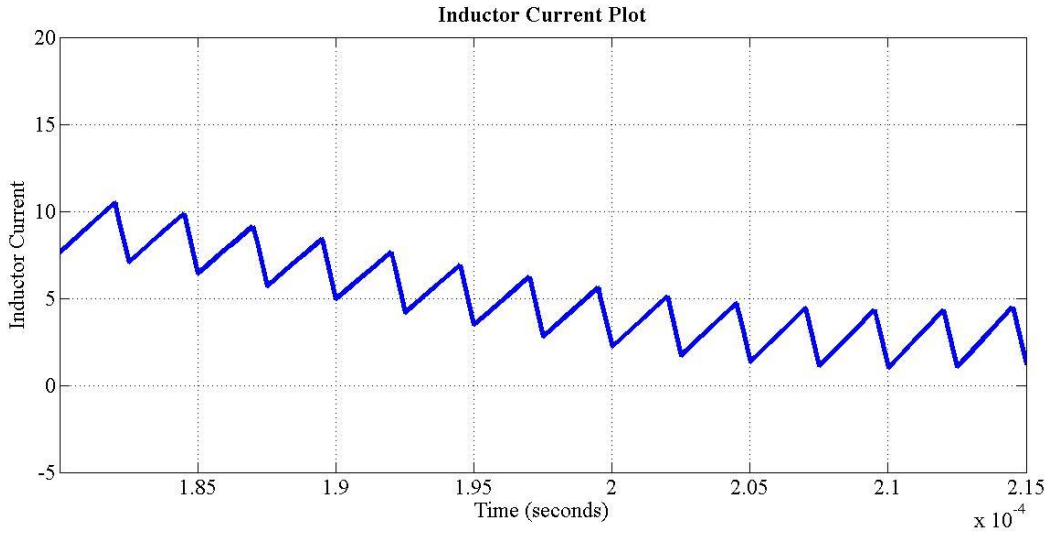

Fig. 5.6 Inductor current of current mode controlled Buck converter

5.1.3 Hardware Output

The hardware setup for the current mode control without slope compensation is shown in Fig. 5.7. The hardware output of the system is shown below.

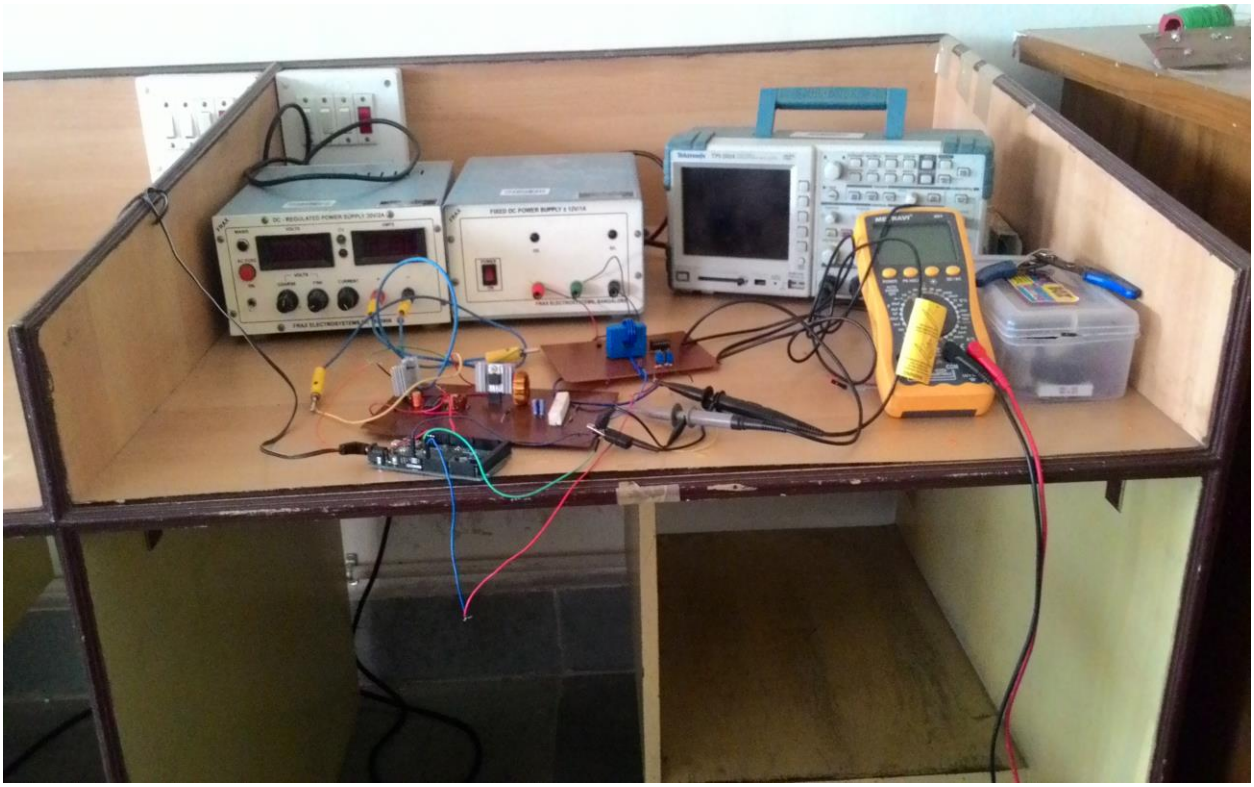

Fig. 5.7 Hardware setup for current mode control

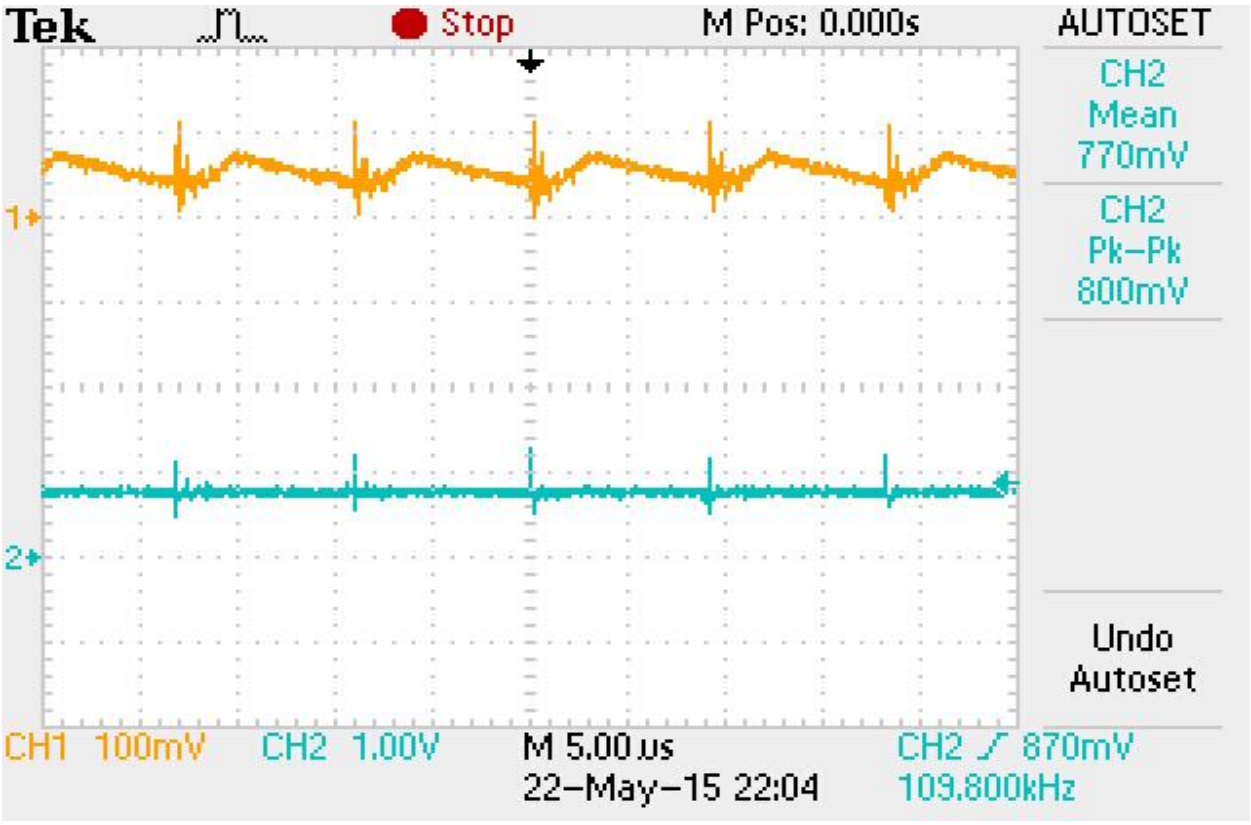

Fig. 5.8 Inductor current and output voltage with 1V reference signal

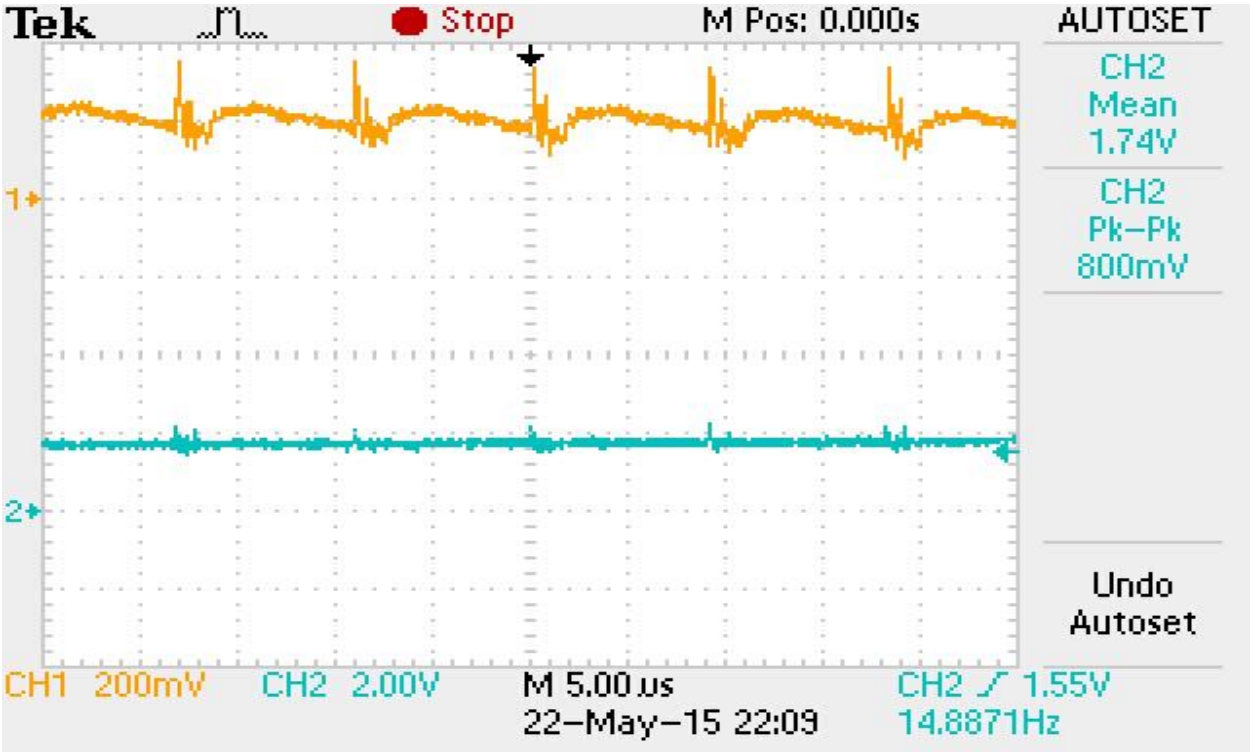

Fig. 5.9 Inductor current and output voltage with 2V reference signal

The inductor current and the output voltage of the current mode controlled buck converter is shown in Fig. 5.8 and 5.9. From the above two figure it can be observed that the output voltage is following the reference signal. The output voltage with AC coupling is shown in Fig. 5.10.

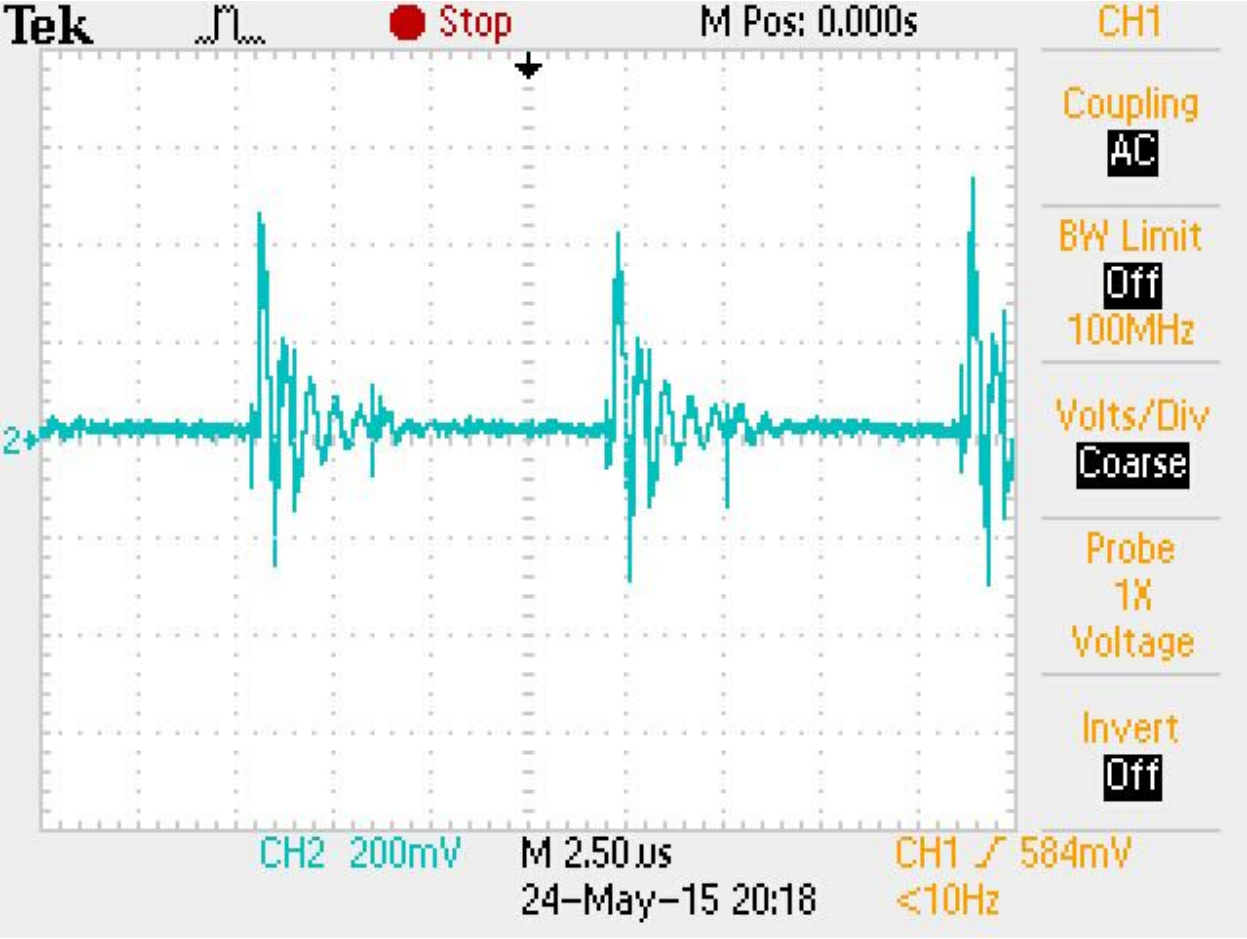

Fig. 5.10 Output voltage with AC coupling

5.2 Auto-tuned PID controller for Fast Transient Response of Buck Converter

Auto-Tuned PID controller is used for fast response time. When the load varies very fast and/or there is a fluctuation in the input voltage then auto-tuned PID controller is required to follow the desired voltage. The transfer function of PID in S-domain is given as:

$$Y(S)=\left[K_p S+K_I\frac{1}{S}+K_d S\right] \tag{5.24}$$

By using the backward difference method i.e. $S=(z-1)/z.T_s$ the Eq. (4.1) is transformed into discrete time domain (Z-domain) and is given below:

$$y(z)=\left[K_p+K_I T_s\frac{1}{\left(1-z^{-1}\right)}+\frac{K_d}{T_s}\left(1-z^{-1}\right)\right] \tag{5.25}$$

In the Eq. (4.2) derivative term is replaced with backward difference function and the integral term is replaced with a sum using rectangular integration to obtain digital PID control algorithm which is given in Eq. (4.3).

$$y(n)=e(n)K_p+\Delta e(n)K_d+\left(\sum_{j=1}^{n}e(j)\right)K_I \tag{5.26}$$

Where,

$$\Delta e(n)=e(n)-e(n-1)\ \ and\quad e(n)=v_{ref}-v_0(n) \tag{5.27}$$

An updating factor $\beta(n)$ is proposed and is given as:

$$\beta(n)=\Delta e_N(n)e_N(n) \tag{5.28}$$

Where,

$$\Delta e_N(n)=\left(e_N(n)-e_N(n-1)\right)\ \ and\ \ e_N(n)=\left[\frac{e(n)}{e_{\max}}\right] \tag{5.29}$$

The gain updating factor $\beta(k)$ will update the controller gains K_p, K_I and K_d in each cycle. The relation between $\beta(n)$ and controller gains K_p, K_I and K_d is given in Eq. (4.7).

$$\begin{aligned}K_p(n)&=K_p\left(K_1\ |\beta(n)|+1\right)\\K_I(n)&=K_I\left(K_2\ \beta(n)+1\right)\\K_d(n)&=K_d\left(K_3\,|\beta(n)|+1\right)\end{aligned} \tag{5.30}$$

Where K_1, K_2, K_3 are three positive constant and K_p, K_I and K_d are controller parameters which can be obtained by any one of the PID tuning methods. By substituting the value of $\Delta e(n)$ from Eq. (4.4) in (4.3) the digital form of auto-tuned PID controller algorithm is obtained and is given as:

$$y(n)=K_p(n)e(n)+K_I(n)\sum_{j=0}^{n}e(j)+K_d\left[e(n)-e(n-1)\right] \tag{5.31}$$

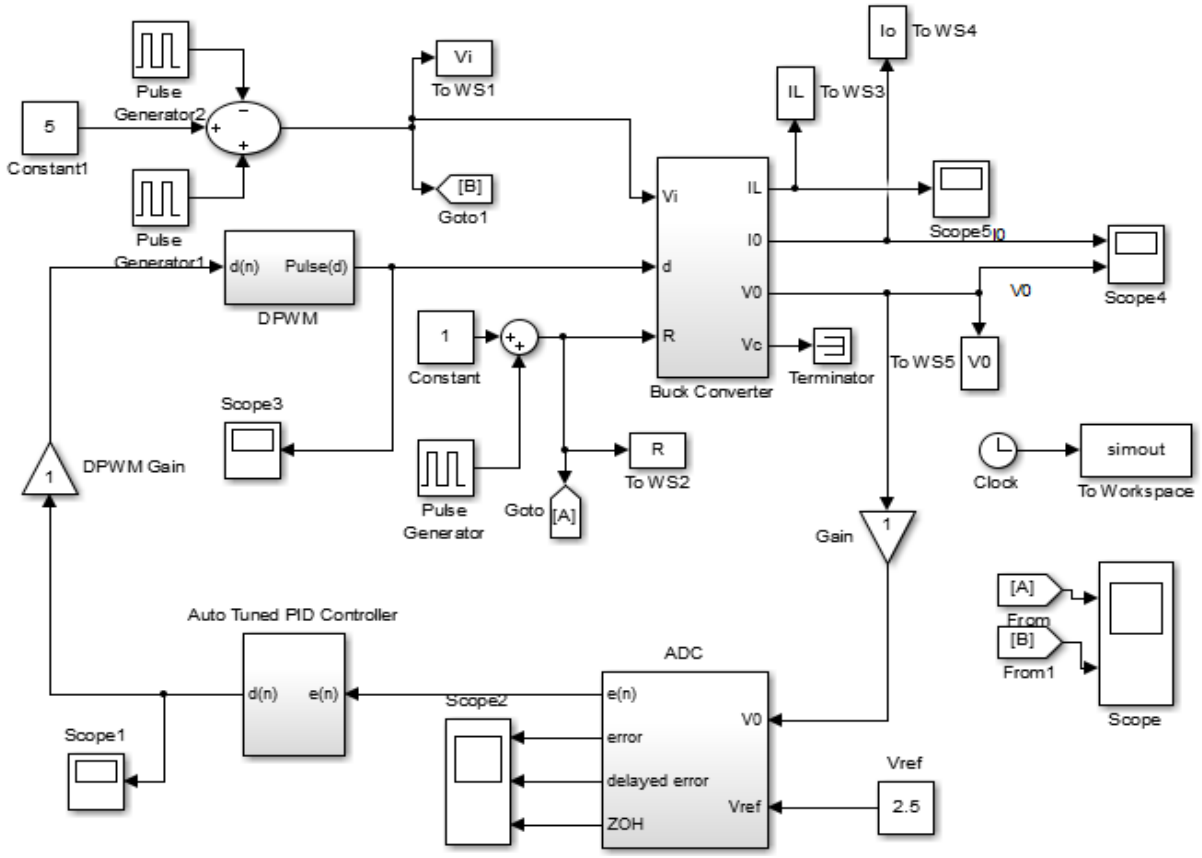

Fig. 5.11 Simulation diagram of auto-tuned buck converter

The nominal voltage of 5V changes to 5.5V, 5V, 4.5V and back to 5V at 3 ms, 6ms, 9ms and 12ms respectively. The converter has load of 1.25 amps and changes to 2.5 amps and back to 1.25 amps in t= 0, 5ms, 10ms respectively corresponding to R=2-1-2 ohms as shown in Fig 5.12.

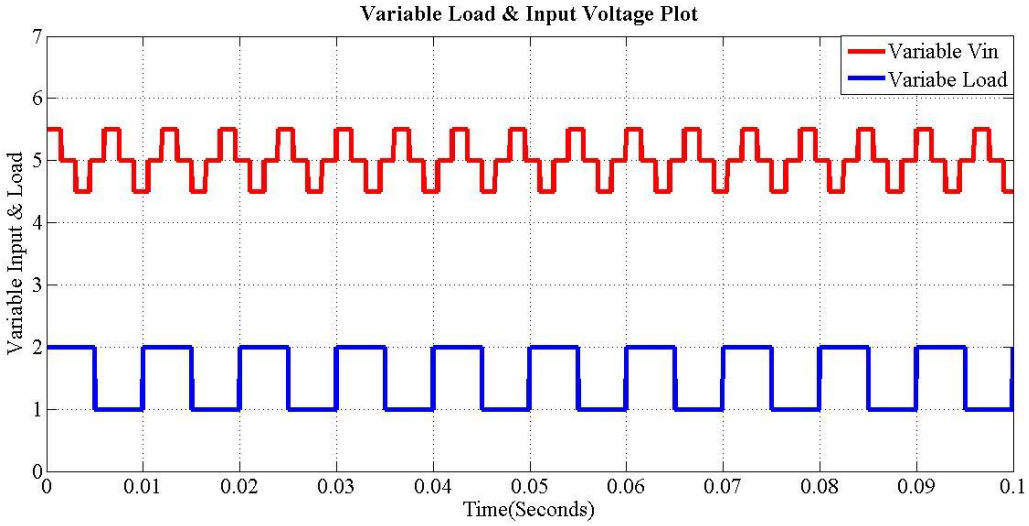

Fig. 5.12 Variable load and input voltage plot

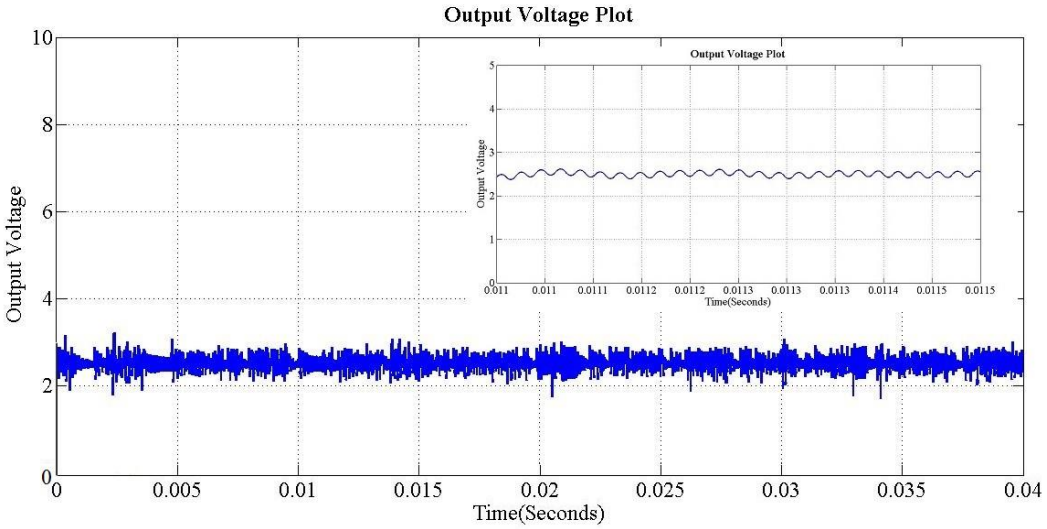

Fig. 5.13 Output voltage of the auto-tuned buck converter

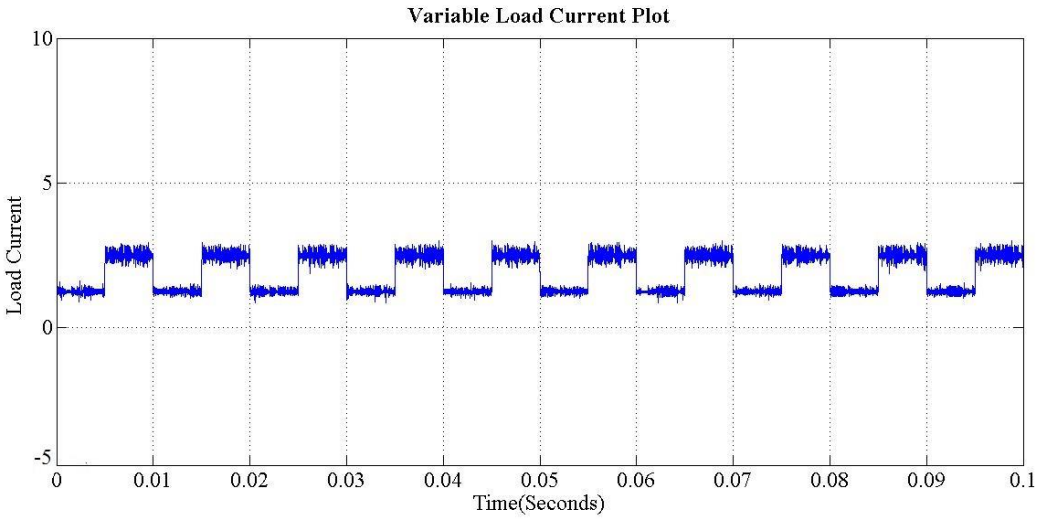

Fig. 5.14 Load current variation of the auto-tuned buck converter

The load current variation and the output voltage of the auto-tuned buck converter is shown in the above figures. From the Fig. 5.12 and 5.14 it can be observed that the load current is changing according to the load variation while the output voltage is almost constant in spite of changing the input voltage and the load.

CHAPTER 6

Conclusion

Different type of controlling of buck converter is presented in the thesis. First of all the small signal modeling of Buck converter and Boost converter is presented to find the transfer function of the converter and a model is proposed for compensator design. In the subsequent chapter digital feedback control is described in which different type of tuning method of PID controller, DPWM, ADC and their effects on the system is discussed. In chapter 4 a voltage mode controlled buck converter is designed. In the voltage mode controlled buck converter the output is stabilizing after 0.8msec of the variation in the load current, if the load current varies faster than the settling time of the system then output will never stabilize. To overcome this problem an auto-tuned PID controller is applied in the voltage controlled system which is able to respond the fast transient response. The output of the system having auto-tuned PID controller is following the fast change in the load current and input voltage. A current mode controlled buck converter is presented to improve the transient response of the system. The current mode control is having faster transient response due to two control loop in the system. The outer loop controls the reference inductor and the inner loop controls the PWM duty ratio. In the thesis current mode controlled buck converter without slope compensation is presented. Normally, in the current mode control slope compensation is required for duty ratio greater than 0.5 but in this system there is no need of slope compensation. The settling time of the output of the current mode controlled buck converter is 0.5msec and that is of voltage mode control is 0.8msec. That means the transient response of the system in the current mode control is improved.

Future Scope

The proposed current mode controlled system requires two voltage sensor since input voltage is also required in the current controller design. A current controller can be designed without using input voltage which will reduce the cost of one voltage sensor.

The proposed controlling approach may be extended to other current control strategies like current mode control without current sensor, average current mode control without slope compensation.

The auto-tuning method can be extended to adaptive tuning of the controller and robust compensator design which is another problem for future work.

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